

# Transceiver architectures for wireless ICs

*Most of tomorrow's wireless offerings will require a digital platform. Understanding and designing transceiver architectures will be mandatory.*

By **Jesal L. Mehta**

In today's world of miniaturization, there is ever-increasing industry pressure to reduce the cost of communication chips. This pressure has driven designers to develop transceivers with higher levels of integration<sup>1</sup>. Achieving the goal of maximum integration between the antenna and data output is not as trivial as replacing external components with on-chip components. Instead it requires a complete overhaul of the front-end design. Traditional radio designs that use excessive bills of materials are seen as less of a solution today where power, size and cost is critical. This has resulted in new radio architectures<sup>2-9</sup> with fewer off-chip components.

Over the past few years, communication systems have been making the transition from analog to digital modulation schemes. Digital modulation provides greater information capacity, higher security, and better quality of communication than analog modulation<sup>10, 11</sup>. In order to improve the modulation and spectral efficiencies, most digital signals

are single side band with suppressed carrier. Over the years many architectures such as the filter method, phase shift method/Hartley architecture and Weaver architecture have evolved to achieve single side-band signals in transmitters<sup>10</sup>. In receivers, these architectures are used to achieve image rejection. Among these architectures, the Weaver and Hartley topologies<sup>10</sup> are more suitable for integration.

This article will provide an overview of recent advancements in receiver and transmitter architectures. It will discuss the system requirements that lead to the selection of a receiver and various topologies will be described. Transmitter requirements and different architectures will also be examined.

## Receiver architectures

The function of a receiver is to successfully demodulate a desired signal in the presence of strong interference and noise<sup>12, 13</sup>.

The received power is a function of the distance and the surrounding environment between the transmitter and the receiver. Thus, the RF power at the input of a receiver can vary from anywhere from a few femtowatts to microwatts, requiring the system to have a large dynamic range. Apart from dealing with large dynamic ranges and noise, a receiver system needs to minimize cost and power consumption. These tradeoffs between the physics and economics make the design of a successful receiver very challenging.

### Receiver sensitivity

One of the key receiver system requirements is its sensitivity. Sensitivity is defined as the lowest available signal power that a receiver can detect while providing an adequate signal-to-noise ratio (SNR) at the receiver output for demodulation<sup>13</sup>. For a system with a digital modulation scheme, the minimum bit error rate (BER) defines the minimum SNR ( $E_b/N_0$ ) necessary for satisfactory reproduction of the desired signal. Top-level system simulations help to evaluate the minimum  $E_b/N_0$  (for a given demodulator architecture) in presence of

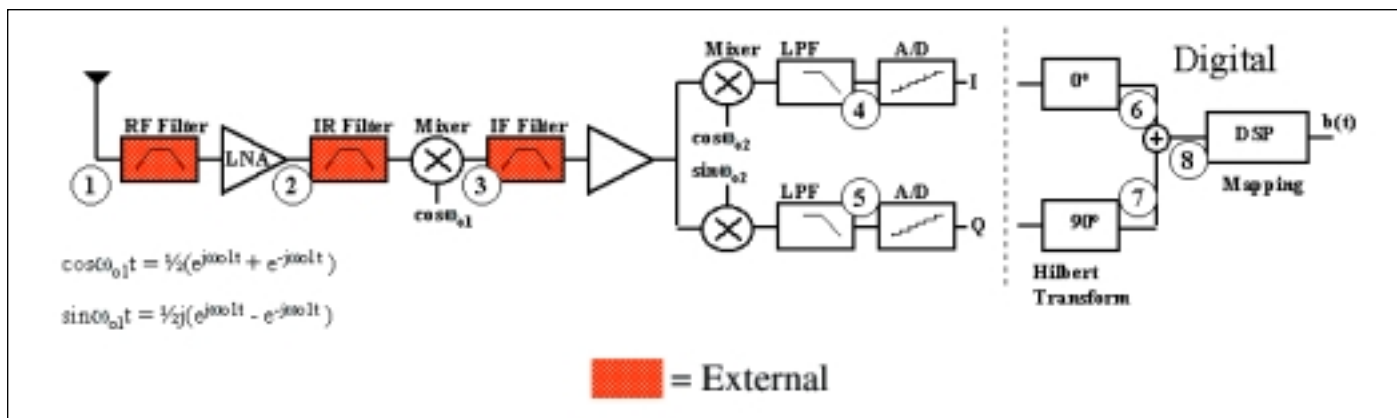


Figure 1. A super-heterodyne architecture.

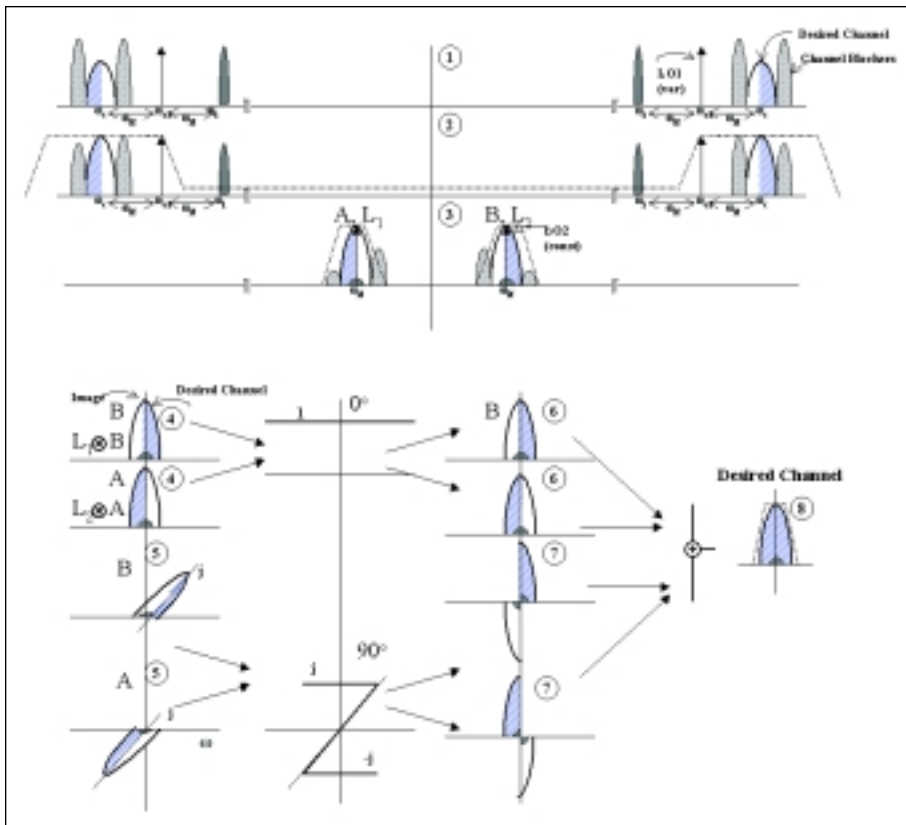


Figure 2. Frequency domain down conversion process for the super-heterodyne architecture.

channel losses such as power law effect and fading. The maximum noise that can be added by the receiver can then be calculated using the simulated  $E_b/N_o$ , sensitivity requirements ( $S_{min}$ ) and channel bandwidth (B) (given in the approved specifications standard).

The equation for minimum allowable receiver noise can be derived from the noise factor definition. Noise factor is expressed as follows:

$$F = \frac{(S/N)_{input}}{(S/N)_{output}} \quad (1)$$

where  $F$  = noise factor, and  $(S/N)_{input}$  and  $(S/N)_{output}$  are the SNR at input and output of a receiver respectively. For successful detection,  $(S/N)_{output} = E_b/N_o$ ,  $S_{input} = S_{min}$  (sensitivity in dBm) and  $N_{input} = kTB$  (available thermal noise power floor); the above equation in decibels becomes:

$$NF = 10 \log(F) = S_{min} (dBm) - 10 \log(kTB) - \frac{E_b}{N_o} (dB) \quad (2)$$

where  $k$  is the Boltzmann constant and  $T$  is the temperature.

Another measure of sensitivity is the minimum detectable signal (MDS). In some literature<sup>13</sup>, MDS is calculated in

terms of noise floor. The noise floor  $P_{nf}$  relationship is as follows:

$$P_{nf} = S_{min} - \frac{E_b}{N_o} = NF + 10 \log(kTB) \quad (3)$$

#### • Receiver selectivity

Another key characteristic of a receiver is its selectivity. Selectivity is defined as the ability of a receiver to satisfactorily extract the desired signal in presence of strong adjacent frequency interferers and channel blockers. In most architectures, the design of a channel select filter at the IF sets the selectivity of a receiver<sup>13</sup>.

A receiver should be sufficiently linear to process the signal with an acceptable distortion level. If the receiver is inadequate in its frequency selection and linearity, it can degrade the desired signal by generating inter-modulation products.

Generally, the level of this distortion determines the maximum power of an input signal that a receiver can process. Third-order distortion is of particular importance in many of the receiver architectures because the intermodulation products lie close to the desired signal. Expressed in terms of third-order input intercept point IIP3<sup>12</sup>, it can be calculated from a two-tone test measurement and the co-channel rejection ratio (CCRR), which is usually specified.

In measuring the intermodulation distortion, power levels of the desired signal,  $P_{sig}$  (dBm) and undesired signals  $P_{ud}$  (dBm – one of which is usually modulated) are known from the specification. The power level of undesired inter-modulation product  $P_{im3}$  that can lie in the desired channel is calculated from the following expression:

$$P_{im3} = P_{sig} - CCRR \quad (4)$$

The third-order intercept of the receiver can be found by:

$$IIP3 (dBm) = P_{ud} + \frac{P_{ud} - P_{im3}}{2} \quad (5)$$

Another useful definition for compression or distortion is the 1-dB compression point,  $P_{1-dB}$ <sup>13</sup>. The 1-dB compression point is defined as a point at which the power gain is down 1-dB from the ideal. It is approximated as follows:

$$P_{1-dB} \approx IIP3 - 10 \text{ dB} \quad (6)$$

#### • Receiver dynamic range

The dynamic range defines the receiver's ability to detect a weak signal above the noise floor and process the large signals with no distortion. The ratio of the maximum signal to the minimum signal at the receiver

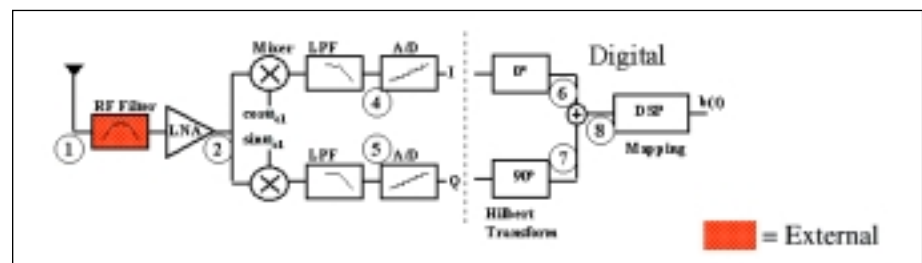


Figure 3. A zero IF architecture.

input defines its dynamic range. It is not unusual to have different dynamic ranges for the same receiver. While  $S_{min}$  sets the lower limit, the upper limit is dependent upon the architecture. Of particular importance are the spurious free dynamic range (SFDR) and the blocking dynamic range (BDR)<sup>13</sup>. SFDR is based on the ratio between the maximum input level for

which the third-order inter-modulation product is below the noise floor and the minimum discernable signal  $S_{min}$ . Using expressions (3) and (5), the SFDR is derived as follows:

$$SFDR = \frac{2}{3} [IIP3 - P_{nr}] - \frac{E_n}{N_0} \text{ (dB)} \quad (7)$$

BDR is defined as the ratio of the upper-bound signal  $P_{-1dB}$  to lower-bound signal  $S_{min}$ . Mathematically, the BDR is expressed as follows:

$$BDR \approx P_{-1dB} - S_{min} \quad (8)$$

The maximum gain of the front-end receive chain is determined by taking into account the largest possible in-band blocker  $P_{bl}$ . This means that the maximum gain is a function of filtering before the gain stages. If the signal required at the input of the demodulator is  $P_{req}$  then the maximum gain is given by the following equation:

$$G_{max} = P_{req} - P_{bl} \quad (9)$$

The largest possible available signal  $P_{sig(max)}$  determines the minimum gain. The equation to calculate minimum gain is:

$$G_{min} = P_{req} - P_{sig(max)} \quad (10)$$

#### • Reciprocal mixing

Another important mechanism that limits the dynamic range of the receiver is reciprocal mixing<sup>13</sup>. The local oscillator (LO) phase noise translates the undesired interferer onto the desired signal band. This results in degradation of SNR at the receiver output. Thus, an oscillator must be designed with low phase noise such that under the worst-case blocking condition it will produce a noise sideband below the receiver noise floor. The required phase noise for the oscillator is given as follows:

$$PN(\Delta f) \left[ \frac{dBc}{Hz} \right] = S_{min} - P_{bl}(\Delta f) - CRR - 10 \log(B) \quad (11)$$

#### Receiver Topologies

Receiver designs have come a long way in terms of receiving and processing signals with minimum cost and power. Integrated circuits have substantially reduced the size, cost and power of the receiver systems. Various receiver topologies have surfaced in recent years, each having advantages and disadvantages.

#### • Superheterodyne receivers

The superheterodyne architecture has become an obvious choice in

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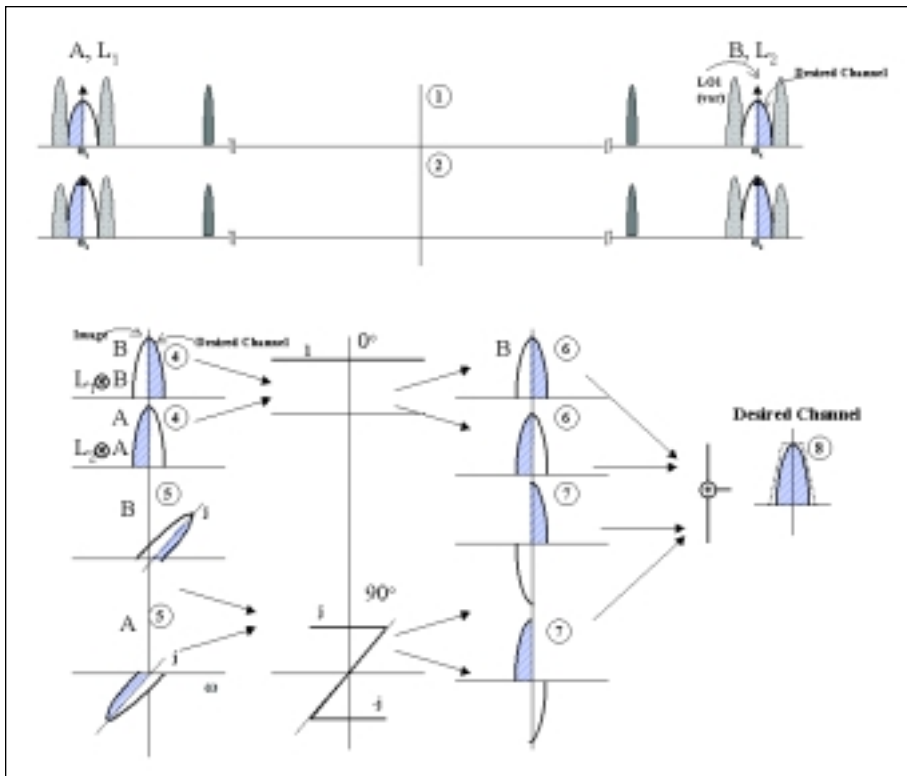


Figure 4. Frequency domain down conversion process for the zero-IF architecture.

receivers since its invention by Armstrong in 1917. Figure 1 shows the superheterodyne receiver dual conversion architecture used in a device designed for 2.4 GHz ISM band applications<sup>14</sup>. The operation and frequency translation of this architecture are well-understood by looking at the radio spectrum at some critical receiver nodes (Figure 2). Here the radio signal is represented by the positive and negative frequencies. An RF filter preceding the low noise amplifier (LNA) attenuates the out-of-band blockers as well as the image. The entire spectrum is then down-converted to a fixed intermediate frequency (IF) using a tunable oscillator. The image is further attenuated to an acceptable level by using an exter-

nal image reject filter before the down-conversion block. The channel selection is normally done using an IF filter following the down-conversion; that reduces the dynamic range requirement for the ensuing blocks. The choice of IF is critical in determining the selectivity and the sensitivity of this receiver. The second down-conversion is usually quadrature in nature to facilitate digital processing of the in-phase and quadrature (I and Q) signals. The figure also shows a conceptual method for generating the desired signal from I and Q signals, using DSP.

Superheterodyne architectures are viewed as the most reliable receiver topology since excellent selectivity and sensitivity are attained by proper

choice of IF and filters<sup>1, 10</sup>. The DC offset and leakage problems do not hamper the receiver performance because of the multiple conversion steps. However, there is some cost penalty in order to achieve adequate performance. External high-Q band-pass filters required for the image rejection and the channel selection increase the cost as well as the size. Since the channel selection is done at the first IF, the local oscillator (LO) requires an external tank for good phase noise performance. All these tradeoffs make it difficult to achieve integration of a transceiver on a single chip.

#### • Zero-IF receivers

The motivation behind eliminating off-chip components has led to zero-IF receiver architectures<sup>2, 3</sup>. Figure 3 shows the block diagram for such a device<sup>14</sup>. It is a direct-conversion (zero-IF) receiver for direct-sequence spread spectrum systems that include phase locked loop (PLL), received signal strength indicator (RSSI) and on-chip filtering. Figure 4 shows the corresponding down-conversion process in the frequency domain. In this topology, the entire RF spectrum is down-converted to DC. A high roll-off low-pass filter (LPF) is used to perform the channel selection. This topology eliminates the image problem and thus avoids the use of external high-Q image reject filters. A quadrature down-conversion generates I and Q signals for further signal processing.

Eliminating off-chip components makes this architecture attractive for integration. Since the power level of the mirror signal is equal to or less than the desired signal, the architecture requires lower image rejection and the image reject filtering can be done on-

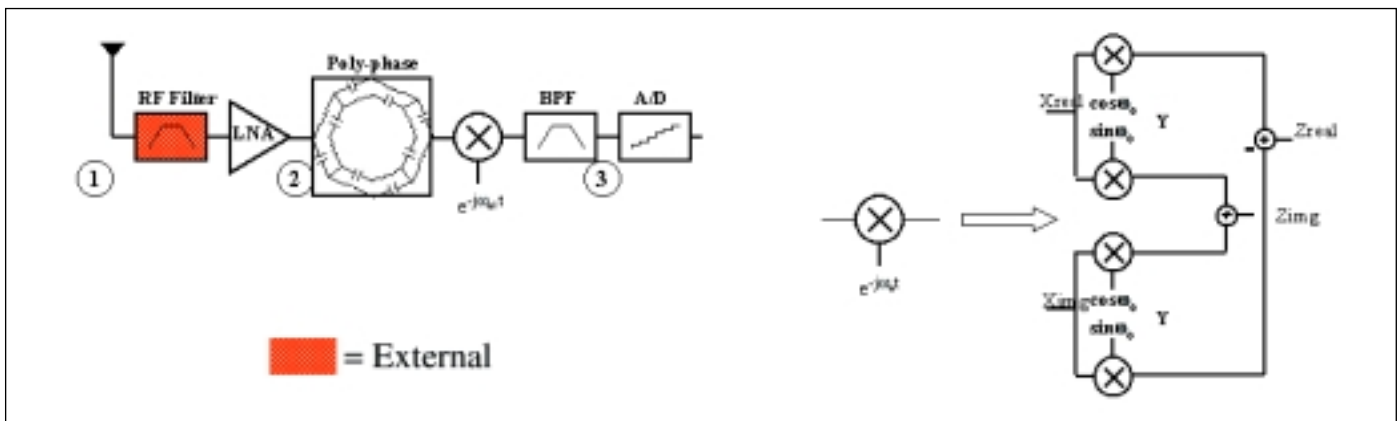


Figure 5. A low-IF architecture.

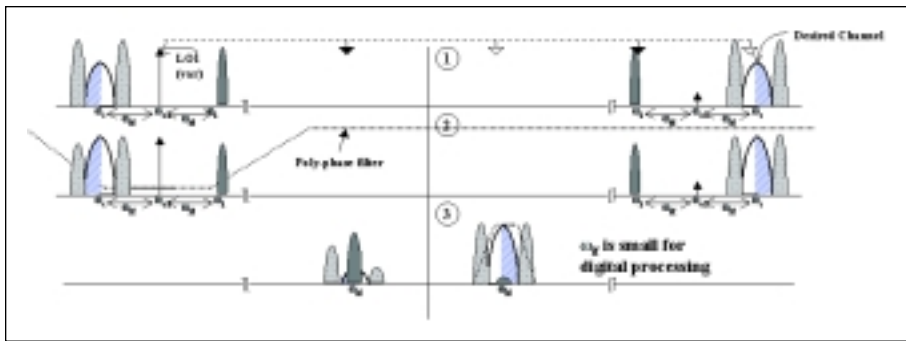


Figure 6. Frequency domain down conversion process for the low-IF architecture.

chip. The process of reciprocal mixing is reduced since only one LO is used to down-convert the signal. Overall, this architecture is excellent at saving cost, die area and power consumption.

However, problems caused by a time-varying DC offset, LO leakage and flicker noise can hamper the

first amplified and filtered with a poly-phase filter that produces a complex signal at its output. This filter acts as an all pass filter for the positive frequencies and a band-stop filter for the negative frequencies. The signal is then down-converted into a quadrature low frequency IF that is typically of the

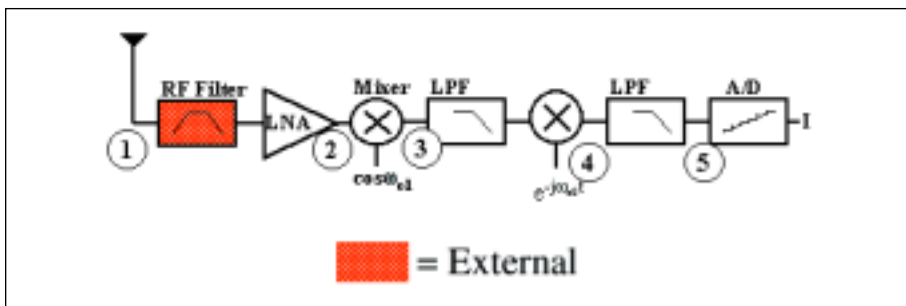


Figure 7. A wideband double IF architecture.

detection of a signal. The DC offset problem can be corrected by using proper digital signal processor (DSP) or auto-zeroing function. A highly linear mixer is used to avoid distortion because no filtering is provided before down-conversion.

This architecture is also more prone to the second-order intermodulation distortion product ( $IM_2$ )<sup>2</sup>. Similar to superheterodyne architecture, this architecture requires variable high-frequency LO to perform the channel selection. This architecture has been successfully used in modulation schemes with little energy at DC such as over-modulated frequency shift keying (FSK) pager system.

#### • Low-IF receivers

The concept of on-chip band-pass filtering has led to low-IF receiver topologies<sup>4</sup>. In this architecture, the IF is at a low frequency (typically hundreds of kHz) thus requiring a low-Q channel select filter. One approach is shown in Figure 5, a 2.4 GHz Bluetooth receiver<sup>14</sup>. The corresponding frequency domain down-conversion process is shown in Figure 6. The RF spectrum is

order of one/two channel bandwidth. This quadrature down-conversion process exploits the mixing properties of a complex mixer. A complex mixer only mixes the positive RF frequencies with a negative LO frequency (vice versa is also true) thus achieving an active image rejection.

Low-IF architectures are suitable for

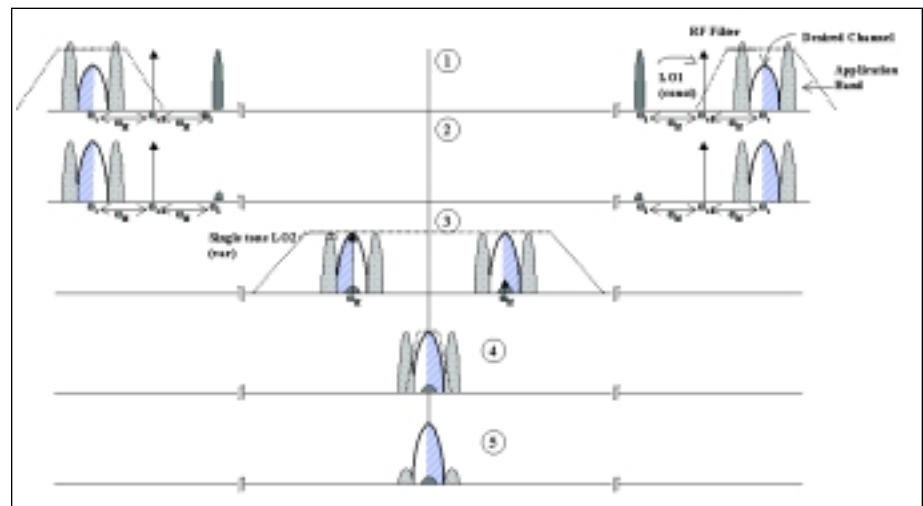


Figure 8. Frequency domain down conversion process for the wideband double-IF architecture.

integration since the image rejection and the channel selection can be done using a low-Q band-pass filter following the mix. Unlike zero-IF architecture, a low-IF is not sensitive to the parasitic DC offset, LO leakage, and  $IM_2$ . Low-IF also provides flexibility for processing the signal in multiple ways. One of the drawbacks of this architecture is its limited image rejection ( $\sim 40\text{dB}$ )<sup>4</sup> due to the on-chip matching between I and Q generators. Implementing an asymmetric poly-phase filter in the signal path to enhance the image rejection introduces insertion loss and causes noise degradation. Without proper pre-filtering, the dynamic range and resolution requirement on an analog-to-digital (A/D) converter can substantially increase. Also, an increase in current consumption results when this topology is used for wide-channel bandwidth application. Again, a variable high frequency LO with good phase noise is needed making synthesizer design difficult.

#### • Wideband double-IF receivers

Recently, UC Berkeley researchers have presented an interesting approach that combines the zero-IF and the heterodyne architectures to optimize power consumption and performance<sup>5</sup>. The functional block diagram is shown in Figure 7. This approach is similar to the superheterodyne that uses multiple IF stages with the first IF at high frequency (hundreds of MHz). Figure 8 shows the corresponding down-conversion process. The entire RF application band spectrum is first down-converted to a high IF using a fixed  $LO_1$ . Since  $LO_1$  is generally selected outside the

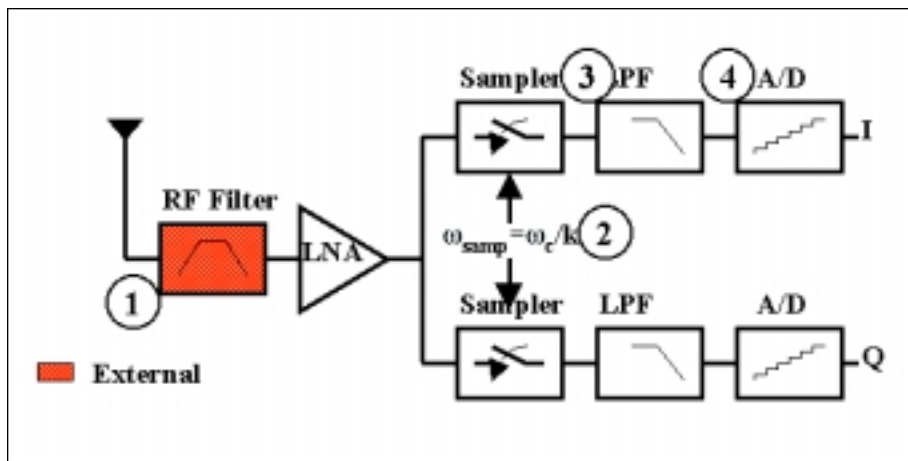


Figure 9. A sub-sampling architecture.

application band, the RF filter following the antenna also acts as an image reject filter. After passing the down-converted signal through a low pass filter, the desired signal is then down-converted to DC using a complex mixer that achieves active image rejection. The desired channel is selected using a variable LO<sub>2</sub>.

This approach is amenable to integration resulting in reduced cost. Furthermore, a fixed LO<sub>1</sub> eases the design of a low phase noise high frequency synthesizer that leads to reduction in power consumption. Since the first IF is fixed at a high frequency, the feedback divider requires a lower division ratio. Hence, the overall phase noise performance of LO<sub>1</sub> is improved. Although the LO leakage problem does not exist, this topology is still plagued by the DC offset and IM<sub>2</sub> distortion. This architecture can also suffer from signal cross talk between IF and RF. A low-pass filter rather than the more current consuming band-pass filter does the channel selection. An adequate image rejection of 55 dB has been demonstrated<sup>6]</sup>. Due to insufficient filtering, six highly linear mixers are used to handle large dynamic range. The DC power consumption can be reduced if the last four mixers are passive in nature.

#### • Sub-sampling receivers

With the emergence of high-speed complementary metal-oxide semiconductor (CMOS) process, several papers have shown sub-sampling systems based on the application of the band-pass sampling theorem<sup>7, 8</sup>. Figure 9 shows the sub-sampling architecture with IF. A sampling circuit replaces the mixer in the zero-IF architecture. Figure 10 shows the down-conversion process in the frequency domain. The RF signal is sampled at the Nyquist

rate of the base-band signal. The band-pass sampling results in a spectral image at the locations given by the following equation:

$$w_i = kw_{smp} \pm w_c \quad (12)$$

where  $k$  is an integer constant,  $w_i$  is the location of spectral image;  $w_i = 0$  for sub-sampling zero-IF architecture, and  $w_{smp}$  and  $w_c$  are the sampling and carrier frequencies respectively. Another example of sub-sampling is demonstrated in<sup>8</sup> and an equivalent block diagram is shown in Figure 11. In this architecture, a noise filter is added to prevent wideband aliasing of noise. Also, successive band-pass down sampling stages are used to select the desired channel. This architecture is more appropriate for narrow-band applications<sup>8</sup>.

This architecture is well-suited for integration, particularly in CMOS technology, because a complex down-conversion process is reduced to a simple

sampling operation. This makes the design of a high-speed switch critical. Since the frequency required for sampling is much lower than the carrier frequency, the oscillator design is simple and less power consuming. One of the major concerns for this architecture is noise aliasing. The noise power is increased by a factor of  $2 \cdot k$ , necessitating the use of an external band-pass noise filter<sup>8</sup>. The jitter on the sampling clock is magnified by factor of  $k^2$ , resulting in interference in the desired channel<sup>8</sup>. Another problem that plagues this architecture is clock feed-through and incomplete settling time of the operational amplifiers. These result in inadequate attenuation of the interferer, and thus require the A/D to have a high dynamic range. Since  $\omega_c$  is proportional to  $\omega_{smp}$ , low-power sub-sampling architectures at higher frequencies are difficult to design.

#### • Digital IF receivers

With the present (CMOS) technology, final mixing and filtering can be performed in the digital domain<sup>9</sup>. In digital IF topology, the IF stage in the super-heterodyne, low-IF and zero-IF architecture is digitized. The use of digital IF avoids imbalance between I and Q, which results in excellent image rejection. This architecture, however, requires a high-performance A/D, thus increasing the current consumption of the overall receiver. The low-IF digital receiver architecture shown in Figure 12 can use a band-pass sigma-delta ( $\Sigma\Delta$ ) converter to decrease the performance requirement of the A/D. The band-pass nature of sigma-delta performs the sam-

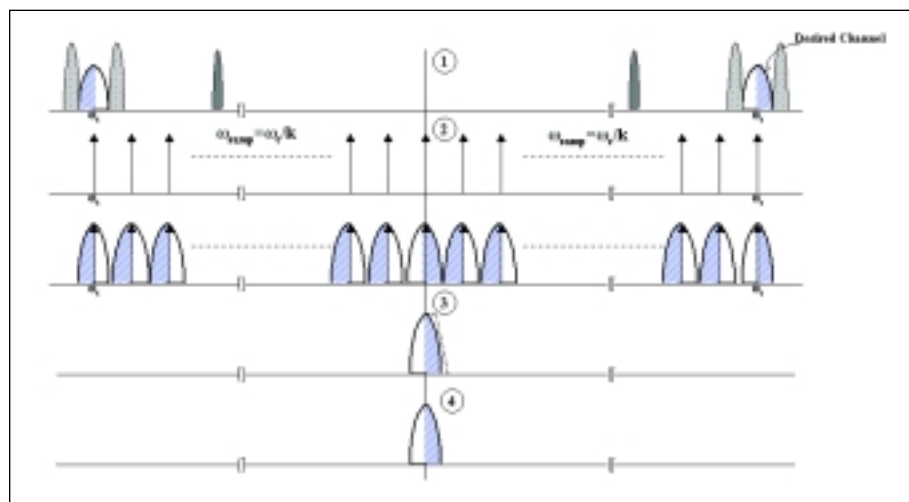


Figure 10. Frequency domain down conversion process for the sub-sampling architecture.

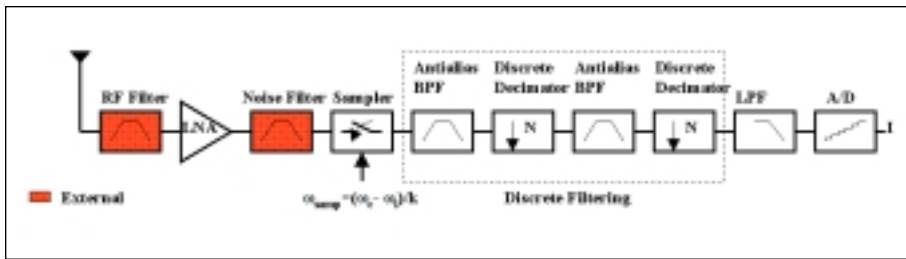


Figure 11. A sub-sampling architecture demonstrated in [8].

pling and the filtering function simultaneously. The potential of digital-IF remains an active research area mainly in design of high frequency A/Ds.

### Transmitter Architectures

#### • Transmitter System Requirements

The purpose of a transmitter is to modulate the base-band data and then up-convert to a carrier frequency  $\omega_c$  (RF). A transmitter also needs to provide sufficient power amplification without distorting the signal or causing undesired emissions in the adjacent channels<sup>15, 16</sup>. The design of a transmitter involves thorough understanding of the type of modulation used. A system architect generally considers tradeoffs among the different modulation schemes in order to determine the best design.

In present wireless communications, the type of modulation used entails tradeoffs between spectral and power efficiencies. The modulation schemes can be broadly classified into “constant envelope” and “variable envelope” mod-

ulations<sup>15</sup>. The constant-envelope as the name suggests has a constant modulated signal amplitude thus allowing amplification by a non-linear power amplifier. Gaussian filtered frequency shift keying (GFSK) signal is an example of such modulation. These modulated signals are more power efficient than spectrally efficient. In most communication systems, the base-band signal is Gaussian filtered so as to vary the frequency shift gradually making it more spectrally efficient. Generally, the

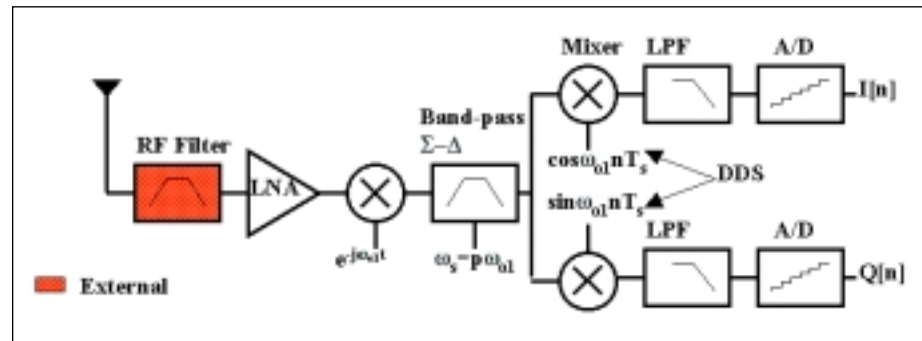
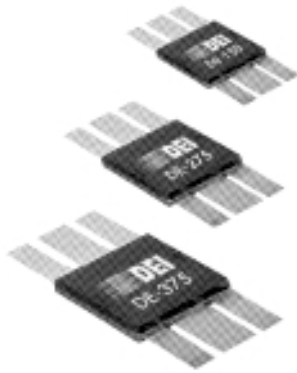


Figure 12. A low-IF architecture with digitized IF stage using band-pass  $\Sigma\Delta$ .

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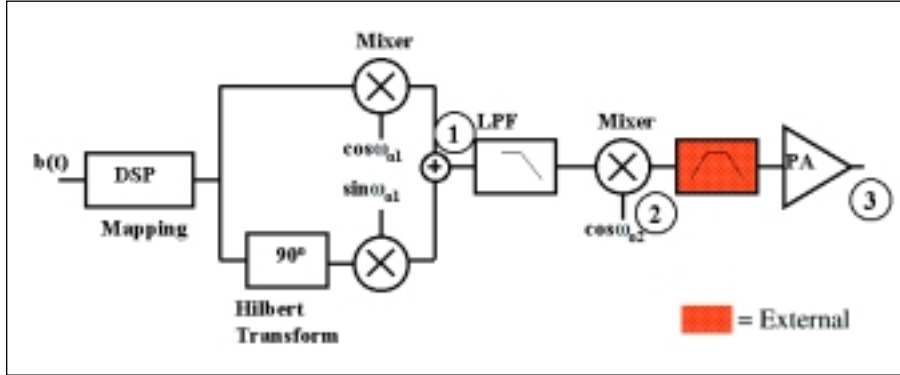


Figure 13. An indirect modulation transmitter.

transmitters for this modulation are required to meet an emission mask specification so that a signal does not interfere with other user's signals. A basic transmitter can be a simple frequency multiplier to up-convert the base-band signal to RF.

Variable-envelope signals such as quadrature phase shift keying (QPSK) have both amplitude and phase variation<sup>15</sup> necessitating the use of linear power amplification. They are spectrally compact, but not very power-efficient. The linearity of such a system is often specified in terms of adjacent channel power ratio (ACPR). ACPR is a measure of the spectral impurity due to non-linear amplification. In order to achieve both power efficiency and linearity, various techniques such as feed forward, feedback, pre-distortion, and linear amplification using non-linear components (LINC) have been proposed<sup>17</sup>. Such signals are up-converted using indirect/direct quadrature modulation schemes. For sake of brevity, a detailed description for each of the modulation schemes is not given.

At this point it is necessary to understand whether the system is time division duplex (TDD) or frequency division duplex (FDD). If the transmit and receive bands are separated by a duplexer the system is called FDD. If the transmit and receive lie in the same band and use an RF switch to perform duplexing the system is called TDD. Generally, low-power, wireless communication systems employ TDD. The total average power delivered to the antenna should take into account losses due to the duplexer or RF switch. The power amplification increases the noise floor of the output spectrum. In transmitter systems that use FDD, the rise of the noise spectrum in the transmitter can cause receiver desensitiza-

tion by the finite feed-through between receive and transmit paths through the duplexer. In addition, the thermal noise of the transmitter must be low enough so as not to degrade the sensitivity of a receiver.

### Transmitter Topologies

In order to share circuits and reduce

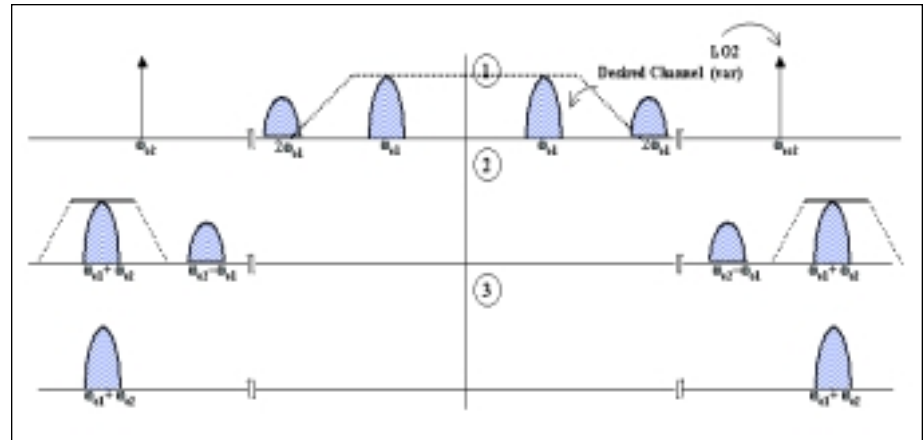


Figure 14. Frequency domain up-conversion process for indirect modulation transmitter.

power consumption, the transmitter and receiver designs are done simultaneously. With proper frequency planning, the transmitter and receiver designs can be optimized to reduce die area and improve performance. At present, various transmitter topologies have been reported<sup>15, 16</sup> for constant and variable envelope modulation schemes. — Indirect modulation transmitters.

The indirect modulation architecture is illustrated in Figure 13. The corresponding frequency up-conversion process is demonstrated in Figure 14. The digital data is first converted to analog and frequency translated by a variable  $LO_1$  to a fixed single sideband IF signal. The signal is then low-pass

filtered to remove  $LO_1$  harmonics and is finally up-converted to  $LO_1+LO_2$  using another mixer. Since the second mixer generates two sidebands, an external filter following the mixer filters out the undesired sideband as well as some additional spurs. The signal is then amplified and transmitted.

This method can be used for both constant and variable envelope modulation schemes<sup>5</sup>. Since the quadrature modulation is performed at IF (a few hundred MHz), excellent matching between I and Q is obtained while consuming little current. In order to meet the spectral mask requirement, two filtering steps are provided for good suppression of spurs and transmitted noise. Indirect modulation prevents injection or LO pulling<sup>15</sup>. LO pulling is a phenomenon in which the LO frequency is controlled by a strong PA signal if both the output and oscillator are at a high frequency.

Although this method is widely popu-

lar, the need for an external band-pass filter for good spurs suppression fails to achieve the present goal of total integration. In addition, this method requires two low phase noise PLLs. Also, an on-

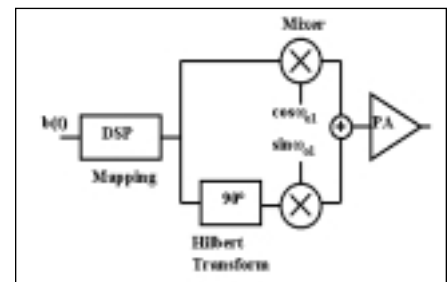


Figure 15. A direct modulation transmitter.

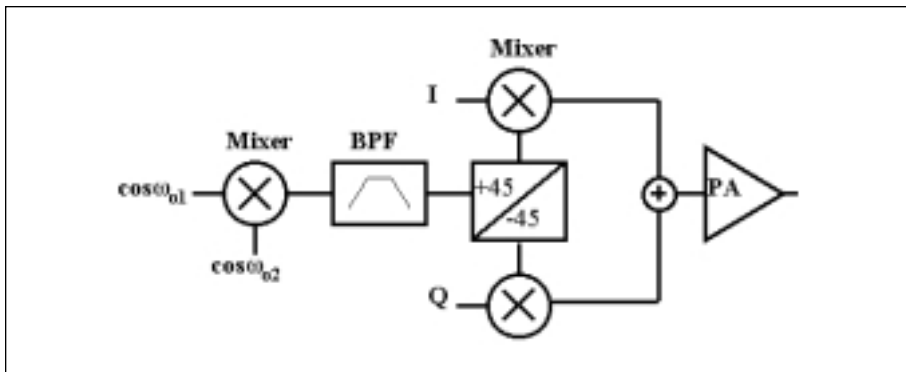


Figure 16. A direct modulation transmitter with offset VCO.

chip filtering provides inadequate suppression of spurs and raises the linearity requirement of the power amplifier<sup>16</sup>. The difficulty in implementing a high-order low-pass filter between the IF and RF stage can lead to an inadequate suppression of spurious signals that are multiples of the IF<sup>16</sup>.

• *Direct modulation transmitters*

Direct modulation architecture, as shown in Figure 15, modulates and up-converts the base-band signal in one step<sup>15</sup>. The hardware consists of two RF mixers and a PLL with the LO running at higher frequency. This architecture offers a high level of integration since image rejection is done actively. The IF-related spurs do not exist at the output since there is no IF.

This architecture uses less hardware compared to indirect modulation, but the need for two mixers operating at RF frequencies can be current consuming. Difficulty in achieving accurate quadrature phase shift at high frequencies gives inadequate image rejection. High-frequency carrier feed through and injection pulling are two potential problems that can occur whenever the oscillator and output are at the same frequency. Although injection pulling can be reduced by proper isolation between the PA and the oscillator, it is difficult to quantify the level of isolation until the entire radio is built.

• *Direct Modulation with offset VCO transmitters*

By mixing two LO frequencies, the LO pulling effect can be alleviated<sup>18</sup>. Figure 16 shows a block diagram for this architecture. The basic operation of this method remains the same as the direct modulation transmitter architecture. In this architecture, the LO frequency is obtained by mixing and filtering two lower frequencies.

This method has the same advantages as direct modulation except that this architecture does not suffer from the LO injection pulling effect. Improper selection of LO frequencies can result in harmonics at the output. The selectivity of the low pass filter following the VCO mixer needs to be good to avoid the impact on the quality of the transmitted signal.

• *Up-conversion modulation loop transmitters*

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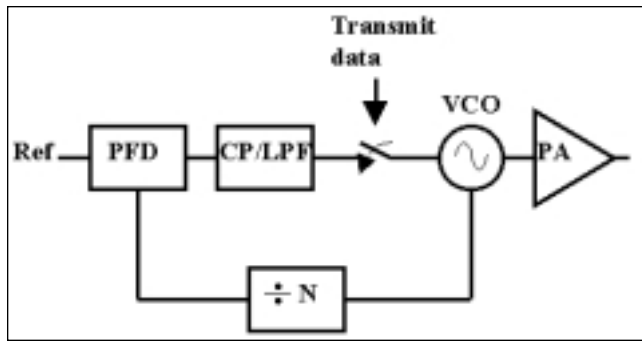


Figure 17. A PLL-based direct modulated VCO transmitter.

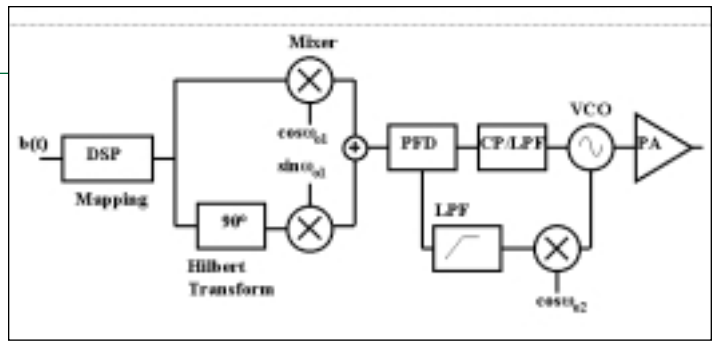


Figure 18. A PLL-based input reference modulated transmitter.

(PLL) as a frequency multiplier makes it an attractive solution for frequency modulation and up-conversion. Under lock condition, a PLL with an input frequency  $F_{ref}$  and a feedback divider  $N$ , has an output frequency  $F_{out}$  given by:

$$F_{out} = N(F_{ref}) \quad (13)$$

cy. This architecture also suffers from injection locking phenomenon, requiring high isolation between the VCO and PA.

- *An input reference modulated transmitter*

A typical PLL-based transmitter is shown in Figure 18. Like the indirect modulation transmitter, the base-band

of ways to generate a modulated reference. One example is to use quadrature modulation in the loop itself<sup>20</sup>. This minimizes phase variation of the signal since a constant  $F_{ref}$  is applied at the phase/frequency detector input. The operation of direct digital synthesis (DDS) at hundreds of MHz is practical due to recent advances in CMOS technology. The concept of a DDS-based modulator driving the PLL is illustrated in Figure 19. Commercial use of this system is hampered by the fine frequency resolution requirement and switching time vs the spurious noise tradeoff.

- *Fractional-N up-conversion*

The fractional-N approach for frequency synthesis has been well-documented in literature<sup>10</sup>. Fractional division allows fine output frequency resolution without lowering the reference frequency. This improves the overall phase noise and settling time of the PLL<sup>21</sup>. If the divide ratio is modulated with the transmit data, then, according to the PLL equation (13), frequency modulation is achieved. Further improvement in spurious noise performance without decreasing the PLL loop bandwidth can be obtained by using phase interpolation, jitter injection, or noise shaping techniques<sup>22</sup>. The latter one uses a  $\Sigma\Delta$  modulator to achieve the noise shaping function.

Figure 20 shows the block diagram of

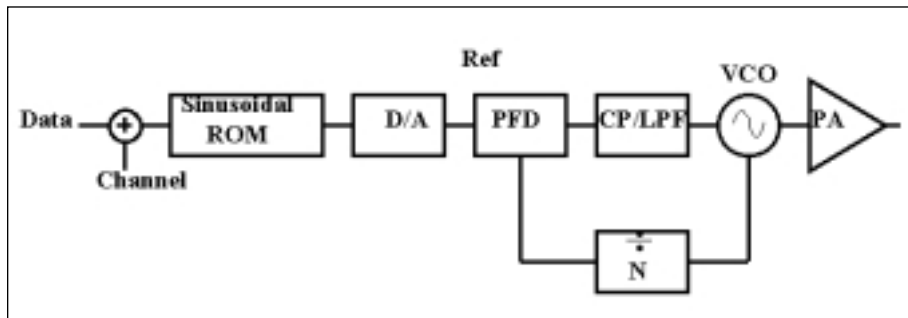


Figure 19. A PLL-based transmitter with input reference generated by DDS.

In order to achieve frequency modulation with up-conversion, either  $F_{ref}$  is modulated or the feedback divider  $N$  is dithered with the transmit data. At present, various hybrids exist for both methods.

- *A PLL-based direct VCO modulated transmitter*

The easiest way to transmit a constant envelope signal is illustrated in Figure 17. In this architecture, the voltage-controlled oscillator (VCO) is directly modulated with the base-band data<sup>19</sup>. Initially the VCO is operated with the PLL to accurately set the carrier frequency. The loop is then broken and the base-band data is applied to the control voltage of the VCO.

This method is advantageous for its high integration and low power consumption. Since the VCO performs both frequency translation and modulation, less hardware is required as well. The biggest disadvantage of this method is that the open VCO tends to drift, resulting in a perturbation of the output frequen-

signal is first translated to IF using a quadrature modulator<sup>15, 19</sup>. A PLL serves to up-convert the IF signal to RF as well as to reduce the filtering requirement on the output signal by the inherent loop action. To relax the fine resolution requirement on  $LO_1$ , the feedback divider is replaced by a down-converting mixer and a low pass filter.

This architecture is simple, low-power and suitable for integration. The inherent narrowband filter provided by the PLL eliminates external band-pass filters. This architecture is only suitable for constant envelope modulation schemes and adds extra hardware since two LOs are required. Injection pulling of the LO is still an issue, requiring higher isolation between the LO and PA.

There are a number

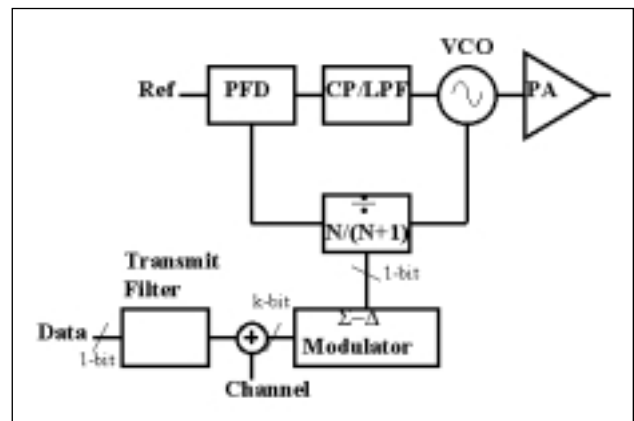


Figure 20. A fractional-N based up conversion loop transmitter.

a transmitter based on the fractional-N method<sup>22</sup>. The base-band data is first filtered by Gaussian shape finite impulse response (FIR) digital filter. The signal is then summed with a channel select divide value that sets the carrier frequency offset. This signal serves as an input to the  $\Sigma\Delta$  modulator whose output changes the divide ratio of the PLL. Thus, a spurious free output signal is obtained by dithering the division ratio. The signal is further amplified to bring the output to the desired power level. The  $\Sigma\Delta$  modulator and dual modulus divider causes noise suppression in the base-band. The quantization noise is pushed to a high frequency and is further attenuated by the PLL loop bandwidth which is low pass in nature. The instantaneous output frequency can be manipulated if the input k bits stream to the  $\Sigma\Delta$  modulator is time modulated.

Apart from having most of the advantages of an input reference modulated based transmitter, higher data rates can be transmitted without lowering the reference frequency. The transmit filter can easily be implemented using an over-sampling counter addressing a ROM lookup table<sup>22</sup>. This fact coupled with not using any mixers or digital-to-analog converters, makes it an attractive low-power, high-integration transmitter architecture. This type of architecture is only suited for constant envelope. However, the architecture described above requires the loop bandwidth of the PLL to be greater than the modulation bandwidth. Using the method proposed in <sup>19</sup>, this tradeoff can be eliminated.

## Conclusion

The article surveyed different transmitter and receiver architectures that are suitable for integration on a single chip. The merits and demerits of each of these architectures were discussed as well. The article also established receiver and transmitter system requirements that determine transceiver performance. In the future, higher integration can potentially lead to the exploration of adaptive transceiver architectures. This will further optimize transceiver performance versus power consumption.

**RF**

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From 1998 to 1999, he was with analog/mixed signal design group at Cadence Design Systems, RTP, NC. As a member of the technical staff he was involved in designs of phase lock loops and other analog circuits in CMOS technologies. Since 1999, he has been with the silicon systems product line at RF Micro Devices Inc., Greensboro, NC as an RF circuit designer. His current interests are in the area of RF/analog circuit designs for wireless and high-speed communication systems, particularly in advanced Si and sub-micron CMOS technologies.

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