

## Mixed signal – spearheading the need for improved design methodologies

*Mixed signal designs may be the great enabler for SoC, but as the designs grow more complex, new verification methodologies must keep up*

By **Henry Y. Chang**

**M**ixed-signal ICs are ushering in a new era of amazing possibilities for systems-on-a-chip (SoC) design. Nowadays it's not uncommon to incorporate hundreds of thousands or even millions of gates onto a single chip, including a sizable peripheral analog circuitry. And because mixed-signal devices feature increasingly complex analog components, it's spearheading the need for improved design methodologies.

Applications for these mixed-signal circuits are numerous, covering an immense segment of the

boxes, DVD players, video game consoles, and high-definition TVs. Complicating matters, many of these consumer devices are on the market for only a few months. Then a new version of the product is rushed out. All of this illustrates the unrelenting pressure on designers to achieve first-pass silicon.

### More workable solutions sought

Typically, a mixed-signal design combines relatively slow analog parts with fast digital portions. Traditionally, the digital circuits are designed in high-level HDL. The analog portion is modeled as a "black-box" using simple digital models. The detail digital circuits and layouts are usually synthesized automatically, while the analog schematics and layouts need to be handcrafted by experienced analog designers using custom design tools. The mixed-signal circuits are then assembled by stitching the circuits (or layouts) of the digital and analog parts together, manually, with minimum or no verifications.

However, because of the ever-increasing complexity of computer, communications and consumer applications, designers must find viable solutions for mixed-signal verification, analog as well as digital.

A tremendous need exists for fast mixed simulation. Chips that combine enormous gate counts of digital logic with critical analog circuits such as PLLs require tools that closely couple the analog and digital simulations.

Because of the global feedback loop and tight integration between analog and digital design portions, mixed-signal verification is essential to ensure the success of the final circuit integration. However, the complexity of these circuits prohibits designers from approaching the challenge with traditional methods.

### Nothing to laugh about

When confronted with a complex analog-mixed signal design, what strategy do you employ? Some designers have been heard to say, "Analog is analog, digital is digital, put 'em together and kneel down and pray." That's an amusing ditty, perhaps, but creating and verifying today's mixed signal ICs is no laughing matter.

Today's mixed-signal circuitry features ever-increasing dual interaction between the analog and digital components, and verifying a mixed-signal chip is critical. It's foolhardy to attempt tape-out without careful verification.

The quality of the integration between analog and digital simulators remains a major hurdle. To combat the inherent obstacles, design teams are using various design methodologies, processes and tools. Not surprisingly, the performance of the analog simulator still creates a huge bottleneck.

By comparison, digital design methods are a virtual slam dunk.

### The growing complexity of mixed-signal designs

Mixed-signal simulations are widely divergent in their difficulty factor. For example, simulating a signal that goes straight through the analog and digital

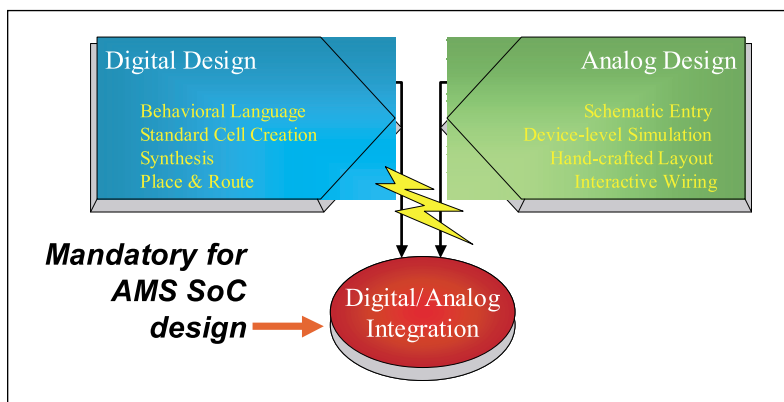


Figure 1. Historically, tools and methodologies for designing digital and analog circuits have been completely different from each other. Design was done in isolation, stitched together at layout and tested after manufacturing.

electronics market. Computers and peripherals incorporate mixed-signal chips into multimedia, audio and video, and networking functions.

Additional uses include wireless communication devices, cellular phones, pagers, and GPS receivers. High-demand consumer applications include set-top

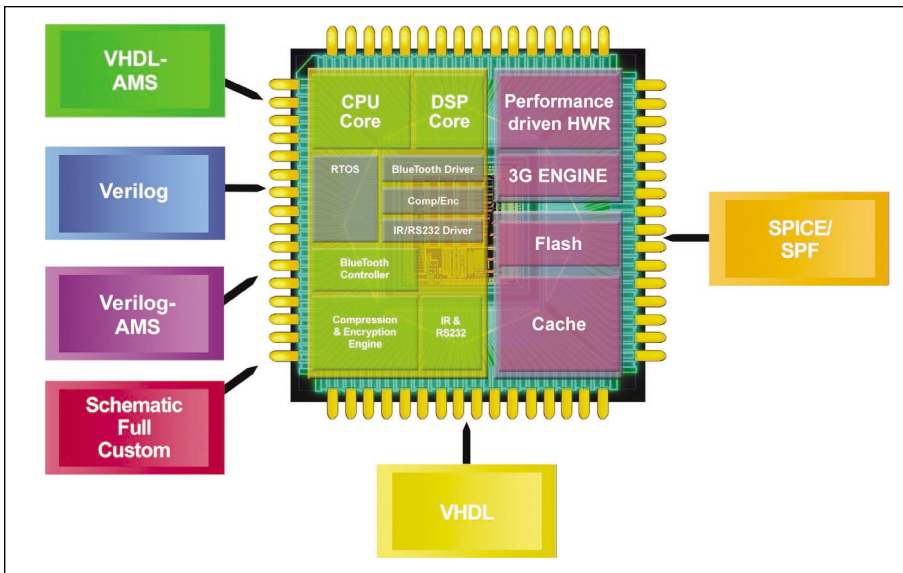


Figure 2. With a multi-level approach to mixed-signal design that is also language-neutral and uses a single netlist hierarchy, designers can freely combine VHDL, Verilog, VHDL-AMS, Verilog-AMS, SPICE and C anywhere in their designs.

sections is not as cumbersome as simulating circuits that join analog and digital portions in a global feedback loop.

Let's take a typical PLL chip from a personal computer, in which the analog portion includes a power management function. When the PC goes into sleep mode, an analog signal is sent to lower down the clock or voltage.

In this example, no feedback is required between the analog and digital parts of the design. Information passes from one portion of the mixed-signal chip to another. So in such a case, it's perfectly feasible to use the traditional method of designing and verifying the chip.

Now let's examine a circuit on the typical cell phone, which features a much more complicated design and includes a feedback loop. The analog portion of the design is closely controlled by the digital, and conversely, the digital portion is closely monitored by the analog.

There needs to be some way of putting together these analog and digital components. In short, a global testing vector is necessary.

In the following paragraphs, we'll present viable alternatives for mixed-signal verification. One approach, top-down design combined with analog behavior modeling languages, provides systematic ways to ensure the success of each design cycle. Through those analog behavioral models, the analog circuits can be brought to a higher level of abstraction, and the overall mixed-signal circuits can be simulated at much higher speed. Another alternative is to couple a digital simulator with a fast-SPICE simulator. With the high-

er speed of fast-SPICE, the analog simulation bottleneck for the mixed-signal verification can be removed.

### Top-down design — analog/digital

Designers are supremely confident that simulating digital portions of mixed-signal circuits will correlate exactly to transistor-level functionality. However, for analog portions, design teams need to create behavioral models that accurately reflect transistor-level operation. Once designers create digital and analog models, chip verification can begin, all within workable time frames.

Designers start from the analog part, only using behavior of circuits to simulate with the digital portion. Designers will divide circuits into functional blocks, write behavioral language for each block, and make sure that every level works.

Each block is logically decomposed, in increasing levels of detail, until the first transistor design is reached. At every point, the analog simulations should run adequately with any partition at any level. This ensures that each partition is accurately moving down toward the implementation level. Such an approach can shave weeks or months off the design cycle, helping companies meet time-to-market deadlines.

It's interesting to note that the analog circuitry of mixed-signal devices usually takes no more than 20% of the IC's total circuitry. Unfortunately, however, analog comprises up to 80% of the test development time. Complicating the issue, few designers possess the experience and skill to create workable analog models. Predictably perhaps, this disparity between analog and digital continues during chip production.

For example, the analog parts of a mixed-signal circuit can take seconds to test, while the digital portion requires a mere fraction of a second.

Furthermore, it is imperative that designers can catch significant real physical effects when building behavior models. For example, designers need to predict various kinds of effects, including timing jitter. If a design team doesn't know there's going to be a jitter effect, how can the team model it?

### Roles of behavioral model libraries

Behavioral model libraries constitute an important and practical tool. As the name implies, a library is an assemblage of models that imitate the behavior of a device. The models are put in place at various levels of abstraction. Each model includes many different parameters, enabling easier customization. In this way, a library with just a few hundred models can help build thousands of applications.

Of course, it isn't always possible to use a model. Some proprietary blocks demand a proprietary model. In these cases, designers need to turn to an analog hardware description language (HDL). A design team can write custom code around an existing model to add needed additional features. Or a company can purchase source code for a library model and use it as a foundation to build a custom library.

### Tapping the power of HDLs

Analog HDLs and behavioral libraries enable system designers to quickly write a block-level system model that can easily be simulated to optimize chip performance. What's more, the task can be accomplished early in the design cycle. Because the system design is written in standard HDL, the design can be used as a live specification to pass down to the transistor-level design. At this point, the design can also be handed off to a design subcontractor.

Verilog-AMS and VHDL-AMS allow designers to create behavioral models of analog and mixed-signal blocks. These are both standard languages, which overcome the impracticalities of proprietary behavioral languages. Analog and mixed-signal behavioral models simulate much faster than gate-level or device-level models.

The Verilog-AMS/VHDL-AMS and AMS behavioral library enable the top-down design methodology for mixed-sig-

## The final alternative: A complete, multilevel approach to mixed signal design

Certainly, gaining the ability to simulate systems at various levels of abstraction allows companies to make the proper trade-offs between design integrity and time-to-market. For those companies willing to make the transition to using a single interface there is the possibility of combining all types of simulation engines from large-signal model simulation, to digital simulation, fast-SPICE simulation and RF simulation into a single environment that uses a single netlist hierarchy and allows designers to freely combine VHDL, Verilog, VHDL-AMS, Verilog-AMS, SPICE and C anywhere in the design. This enables both top-down design and mixed-level simulation for bottom-up verification. In this way, the digital portions of the chip can be analyzed with appropriate methods at the same time that the analog portions are being simulated using SPICE or Fastfast-SPICE, thus allowing both portions of the chip to be simulated accurately in a time-efficient manner. A fully integrated solution allows a large design team to validate the mixed-signal SoC at various stages of the design cycles in a consistent verification platform. Figure 2 presents a complete, multi-level approach to mixed signal design.

nal designs. In this methodology, full-chip mixed-signal SoC verification can be performed from higher to lower levels of abstraction, and from early to later stages of the design cycles. With this methodology, mixed-signal architectural or integration errors can be identified

and corrected early in the design cycle and overall design productivity and time-to-market are greatly improved.

However, the biggest hurdle for adopting this design flow is the methodology change, since the analog design traditionally uses bottom-up design

methodology. Circuit blocks are first designed in transistor level, and then gradually stitched together to create larger circuit blocks. To change this bottom-up methodology to top-down, the analog designers need to change the way they were trained in circuit design.

This obstacle is in addition to learning how to describe analog circuits in Verilog-AMS or VHDL-AMS, instead of in transistors. Nevertheless, from the experience of many mixed-signal design companies who have the determination and resource to adopt this methodology, the huge benefit in productivity gain is definitely worth the growing pains.

### SPICE vs. "Fast-Spice"

There are two basic types of analog simulation—the tried and true SPICE, which has been in use for more than three decades or the relatively new version called Fast-Spice, which has only been around for about seven years or so. The benefit of Fast-Spice, of course, is the speed and capacity improvement over traditional SPICE. It has been

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successfully adopted to help the verification of memory and many types of analog circuits, where circuit sizes are large and the simulations take days or weeks for traditional SPICE. Another benefit of Fast-Spice is that designers don't necessarily need to change methodologies. Design teams can continue to use the same design verification flow that uses Verilog/VHDL for

the digital-only verification and SPICE/Fast-SPICE for the analog only simulation. The mixed-signal verification is an add-on to this design flow at the end of the design cycle for chip assembly. With the higher simulation speed and less impact to the design flow, the mixed-signal simulation with Fast-Spice provides a solution much easier for most design teams to adopt

### No magic bullet exists...yet

At the moment, there is no perfect solution to the considerable challenges presented by mixed-signal system design. Companies need to carefully weigh several important factors: "Is the design simple enough to proceed in a traditional manner?" "How much are we willing to invest in learning top-down design?" "What approach makes good business sense?"

Certainly, gaining the ability to simulate systems at various levels of abstraction allows companies to make the proper trade-offs between design integrity and time-to-market.

Another key consideration is choosing a technology partner. It's important to establish solid relationships that foster an environment of trust and openness. The interactive processes involved in mixed-signal design are helped along by long-term collaboration.

When selecting a vendor for analog modeling it's important to select one that shortens the learning curve and helps overcome obstacles along the way. Onsite help is often critical.

### The assessment

In conclusion, there are many strong business reasons that compel a switch to top-down design, behavioral modeling and bottom-up verification. It can't be stated enough: Ever-increasing chip complexity and time-to-market pressures continue to mount. And the pressures will only intensify as technology continues to advance.

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### About the author

Henry Y. Chang, Ph. D., is the director of marketing, analog/mixed-signal product group. He received his Ph. D. from the University of Washington, Seattle, in 1994. The focus of his research included analog circuit simulation, timing simulation and timing modeling. After his graduation, Henry co-founded a startup company, Anagram Inc, in 1994, where he was the principle architect of the Fast-Spice simulator. Avanti acquired Anagram in 1996 and Henry managed the R & D team for Star-Sim (ADM). Later, he managed Avanti's Circuit Simulation Product Line. He can be reached at [henry\\_chang@mentor.com](mailto:henry_chang@mentor.com).