

Designing a high-speed modem for microwave, satellite communications

Developing a DSP-based modem for demanding high data-rate transmission offers a number of design challenges. But the benefits will be well worth it.

By A. Guidi, P. McIlree and John Stannard

The need for high data-rate transmission presents significant hardware design challenges. A flexible DSP-based modem project for high data-rate transmission applications has been jointly developed by the University of South Australia and JNS Electronics Pty. (Melbourne).

The need

Because Australia has tight spurious emission specifications for allocated channel bandwidth, spectral efficiency was the major objective of the modem design. Various methods were used to achieve high

spectral efficiency, minimizing spurious emissions outside allocated frequency bands of operation. A second objective for this project was to address microwave terrestrial and satellite communications.

As the article progresses, the modem function blocks are developed and each block is discussed.

Let's modulate

The modulator processes the transmitted data differently, depending on the choice of modulation and coding schemes. The chosen modulation scheme depends on whether power efficiency or spectral efficiency is more important.

Spectral efficiency ($>2\text{bits/s/Hz}$) is achieved with high-order modulation schemes such as eight-phase shift keying (8PSK) and 16-quadrature amplitude modulation (16QAM). The output of the modulator is a bandpass signal centered on an intermediate frequency (IF).

The upconverter performs translation of the signal from an IF to a desired transmit (TX) IF. For microwave terrestrial link communications, the final TX frequency is L-Band. For satellite communications, the upconverter provides a 70/140 MHz transmit IF interface for satellite earth station applications. The channel adds noise to the signal and, depending on the application, the signal can be distorted a number of ways. Microwave digital radio is susceptible to frequency-selective fading because of the interference of multipath signal components, while satellite links are more susceptible to signal attenuation because of climactic effects such as rain. The downconverter operates in reverse from the upconverter, mixing the signal down to an IF. The demodulator is responsible for receive filtering and sampling the wanted signal. Once the signal is sampled, it is processed digitally to estimate and remove carrier phase and symbol timing offsets.

The digital modulator

• Baseband I/Q modulator

Figure 2 shows a previously successful design of a high-speed modulator developed by the Satellite Communications Research Centre (SCRC)¹. The figure shows an oversampling factor of four times per symbol period. The mapper generates in-phase and quadrature (I/Q) components. Each component is filtered by a digital finite impulse response (FIR) filter implemented using a look-up-table (LUT) in a read-only memory (ROM). The LUT contains pre-computed convolutions of the input sequence with the filter coefficients. The purpose of filtering is to shape the transmitted pulse (Root Nyquist $\alpha = 0.4$) to eliminate intersymbol interference (ISI) between adjacent symbols. After digital-to-analog conversion, the signal is mixed up to an IF.

The problem associated with this implementation is that its performance depends on the accuracy of the analog quadrature modulator. Any amplitude and quadrature phase imbalance results in a degradation in system performance². This factor becomes more important as the order of the modu-

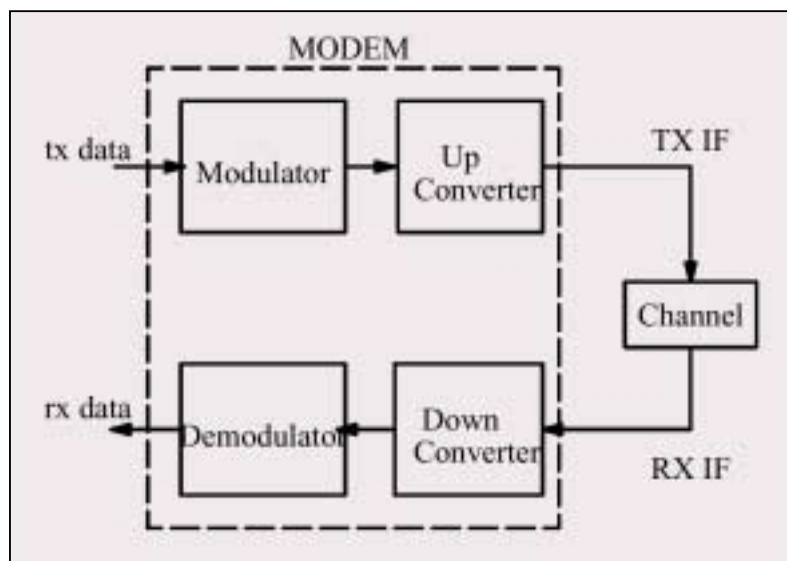


Figure 1. The communication's system modem block diagram.

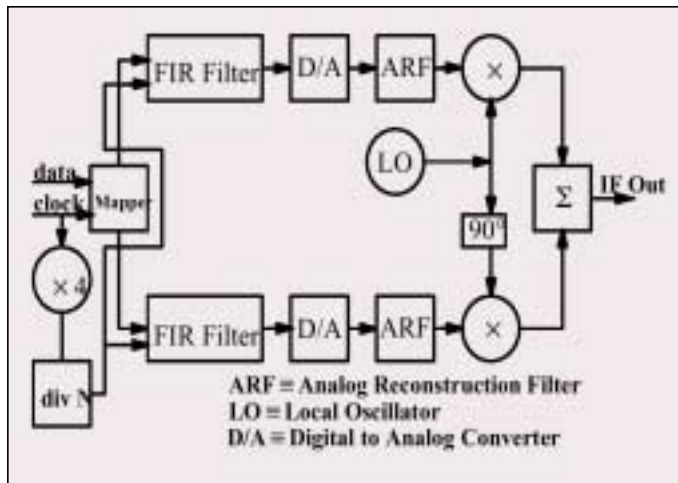


Figure 2. A baseband I/Q modulator.

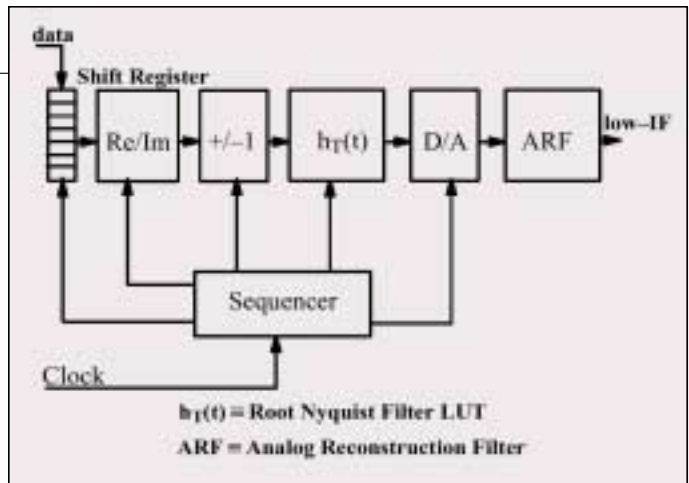


Figure 3. A digital low-IF modulator.

lation scheme increases. Schemes such as 8PSK and 16QAM are much more sensitive to quadrature modulator imbalance than binary phase shift keying (BPSK) and quaternary phase shift keying (QPSK).

• *Digital IF modulator*

To avoid the problems with the quadrature modulator mentioned in the previous section, shift the signal from the baseband digitally and reconstruct the bandpass signal centered on a low IF³.

Because the initial upconversion is performed in the digital domain, it eliminates problems associated with the quadrature modulator. The digital upconversion process is simplified by exploiting a relationship between the low IF and the sampling rate. This relationship is given by:

$$f_{\text{sampling}} = 4 \cdot f_{\text{low-IF}} \quad (1)$$

As a result, the frequency upconversion simplifies interleaving in-phase and quadrature components, with inversions of the data occurring for every second I and Q sample. Also, if the oversampling factor is equal to four, the low-IF frequency equals the symbol rate. One other advantage of digital IF modulation is that only one digital-to-analog (D/A) converter is required. Figure 3 gives a proposed implementation of the low-IF modulator⁴.

• *Hardware implementation*

To keep the low IF and hence, all bandpass filtering stages as fixed as possible, the oversampling factor is doubled for every halving of the symbol rate. Therefore, the lowest symbol rate will result in the highest oversampling factor. The greater the oversampling factor, the greater the number of lines required to address the transmit filter LUT⁴.

Techniques can be used to reduce the size and speed of the ROM required.

For example, a field-programmable gate array (FPGA) can be used to generate the addresses for the LUT. The LUTs are implemented using EPROM/PROM technology, eliminating the extra interfacing required to support RAM technology. The low-IF modulator and the baseband I/Q modulator are similar in terms of required components.

An I/Q design requires two D/A converters, whereas the low-IF design requires only one. The low-IF design does not require a combiner, 90° phase splitter or additional mixer. However the low-IF design generally requires more memory. This factor is offset by the continual decline in cost of memory components.

Up/down conversion

The upconverter consists of two stages: a UHF upconverter to a common IF, followed by a microwave or satellite IF converter (see Figure 4). The upconverter meets Australia's tight spurious emission mask specifications.

Another design feature of the up/down converter minimizes phase noise so that modem performance is not degraded. Also, no IF filtering may introduce significant amplitude and group delay distortion. The choice of a common UHF frequency for microwave radio and satellite applications allows simplification of bandpass filtering design for both frequency converters.

The specifications for microwave radio out-of-band emissions are established in Australia by the Spectrum Management Agency (SMA). The SMA states that the maximum spurious outside the transmitted channel bandwidth is to be -50 dB measured relative to an unmodulated carrier⁵. The upconverter design aims to meet this figure further by 10 dB. The upconverter includes a surface acoustic wave (SAW) filter for close in reduction of spurious emissions.

Another factor influencing the design and cost is the allowable frequency offset. CCIR recommendations determine the maximum frequency offsets allowable in the design. None of the phase-locked loops (PLLs) present in the up/down converter may introduce significant phase noise, such that system performance (measured in terms of bit error rate and spectrum usage) is degraded. The up/down converter provides excellent phase-noise performance by locking all PLLs to a single frequency reference. The stable frequency reference ensures long-term stability and accuracy of the up/down converter.

The frequency plan of the downconverter is identical to the upconverter. It uses the same UHF interface for satellite and microwave radio as the upconverter. The downconverter also incorporates automatic gain control (AGC) and automatic frequency control (AFC).

Digital demodulator

• *Baseband I/Q demodulator*

Figure 5 shows the front-end design of a baseband demodulator applicable for high-data-rate (Mb/s/sec) communications. The signal is shifted down to nominal baseband by an analog quadrature downconverter. The I/Q demodulator is subject to the same amplitude and phase imbalance as the baseband I/Q modulator. The signal plus noise is filtered using a filter having a frequency response characteristic that is an approximation to the Root Nyquist response. One such filter is an equalized low-pass Butterworth. After filtering, the signal is sampled and the digital outputs are processed to remove symbol timing and carrier phase offsets. The front end in Figure 5 has been previously used by the SCRC and incorporated with the modulator described in the *Baseband I/Q modulator* section¹.

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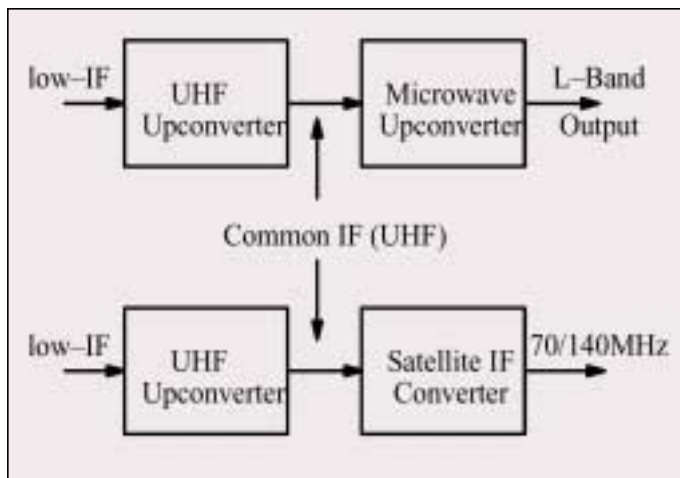


Figure 4. An RF upconverter.

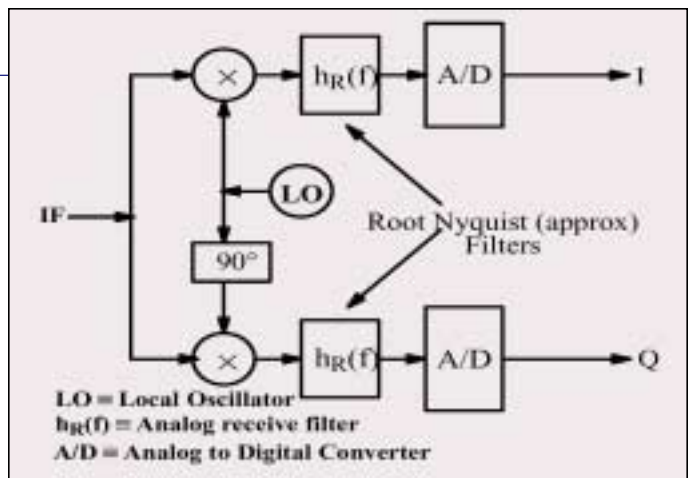


Figure 5. A baseband I/Q demodulator.

Digital IF demodulator

The front end of the digital low-IF demodulator is shown in Figure 6. The downconversion process in the demodulator is the same as that in the modulator in that it exploits the same relationship between the low IF and the sampling rate¹. The difference between the two is in hardware implementation. One difference between the two architectures shown in Figures 5 and 6 is that, instead of mixing the signal down to baseband, the signal is mixed down to a low IF.

Selection of a suitable analog-to-digital (A/D) converter to sample the wide-band signal centered on the desired low IF is important. The A/D must provide sufficient bandwidth and signal-to-noise ratio so that performance is not degraded over the frequency range of operation. Another difference between the two architectures shown in Figures 5 and 6 is that in Figure 6, the receive filtering is performed in the digital domain after sampling. This has advantages because the TX and receive filters can now be perfectly matched. Therefore, in a noiseless environment, no inter-symbol interference (ISI) would occur between adjacent symbols. Another advantage is that digital FIR filters have constant group delay.

• Demodulator synchronization

One of the most important functions of the demodulator is to perform both carrier phase and symbol timing synchronization.

• Carrier phase synchronization

The purpose of carrier phase synchronization is to correct for any instantaneous phase offset in the received signal. The instantaneous phase offset needs to be estimated to rotate the transmitted constellation back to its original position.

A QPSK constellation with a phase offset of a few degrees is shown in Figure 7. The white points correspond to the

transmitted constellation location, while the black points correspond to the signal with a phase offset. Phase offsets result from differences in the instantaneous phase between quadrature oscillator signals in the up/down converters and carrier phase offsets induced by the channel.

Phase recovery algorithms are typically implemented as first-order digital phase-locked loops (DPLLs). The loop bandwidth is set so that the maximum frequency offset likely to be present can be tracked out.

• Symbol timing recovery

The purpose of symbol timing recovery is to adjust the phase of the sampling clock so that the signal is sampled at a point corresponding to maximum eye opening. Due to variations in the transmission channel, the point of maximum eye opening does not remain constant between symbols; therefore, a PLL is required to track this point. Symbol timing can be achieved with feedback or feedforward schemes. For high-speed applications, feedback schemes are the most common⁶.

With feedback schemes, the output of a timing detector generates a signal that passes through a loop filter. The output of the filter is a voltage proportional to the timing error, which adjusts the frequency of a voltage-controlled crystal oscillator (VCXO) or numerically controlled oscillator (NCO) that samples the received signal. The PLL is implemented in a hybrid (analog/digital) form. For further information on modem synchronization techniques, refer to [3].

Hardware implementation

The high data rates that need to be supported with the low-IF demodulator result in the use of specialized hardware architectures to perform DSP functions. For data rates in the tens of Mb/sec, standard reduced instruction set computing (RISC) microprocessor-

based DSP devices cannot be used because their maximum throughput and cycle times are too slow. Instead, algorithms are implemented in application-specific integrated circuits (ASICs) and FPGAs, which are effective in minimizing product development cycles.

Digital filtering is achieved with FIR ASICs having the flexibility to support data rates from 5 to 40 MHz. These filters can be configured as interpolators (increase sampling rate) and decimators (decrease sampling rate). For this application, the FIR filters are configured as decimators to reduce the oversampling factor to 1 sample/symbol.

Decimating is required because the chosen symbol timing and carrier phase recovery algorithms operate using only 1 sample/symbol⁷. The filters are controlled with a simple, external-state machine implemented within an FPGA. A development system is currently being prototyped and tested. The process of downconverting the signal from a low IF to baseband is also carried out in the FPGA. The FPGA will output two streams (I and Q), which will then be filtered using the ASICs described previously.

Figure 8 gives a general block diagram for a proposed architecture to achieve carrier phase synchronization and symbol timing recovery. The diagram shows feedback schemes for timing and phase synchronization. Because of the high-speed requirements, the functions of timing and phase offset estimation are performed in LUTs using ROM. Field application of working systems have proven that the optimum detector and idea level of quantization for each signal have been achieved.

Other system considerations

• Forward error correction (FEC)

The baseband I/Q modem provided no

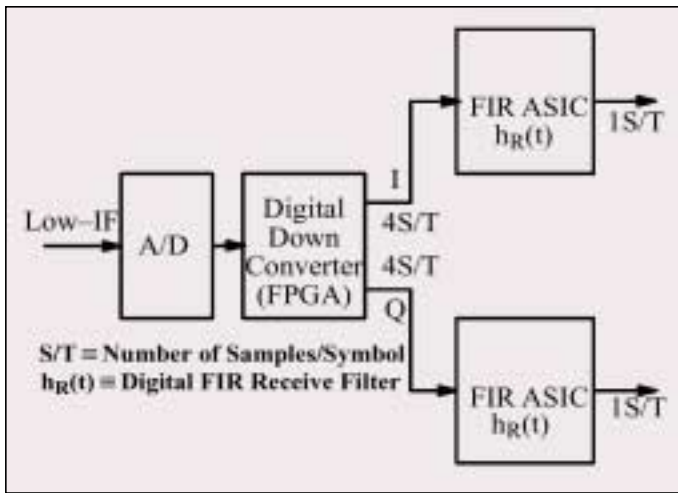


Figure 6. The digital IF demodulator.

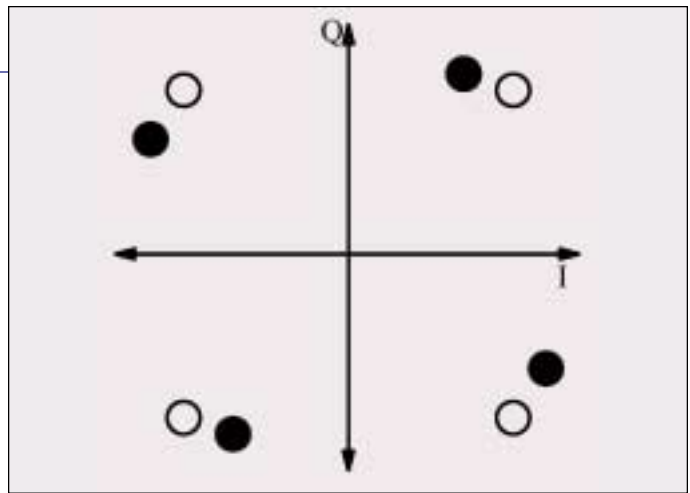


Figure 7. Phase rotated QPSK constellation.

FEC to detect and correct errors within the data stream. The low-IF modem will allow for various FEC coding options. Not only does FEC provide coding gain, but it can also reduce spectral regrowth from the non-linear characteristic of a high-power amplifier (HPA) when operating at or near its saturation region to provide maximum power efficiency.

Along with the uncoded schemes, the low-IF modem will provide FEC coding based on Reed-Solomon codes and

almost constant envelope (ACE) modulation coding^{8,9}. Some of these FEC schemes will provide great coding gain (5 dB for 16QAM at a BER = 10^{-8}), but will provide poor performance in terms of spectral regrowth when subject to non-linearities.

Modulation coding schemes do not provide coding gain (-0.7 dB for 8PSK at a BER = 10^{-8}), but have an excellent response when subject to non-linearities. Some schemes will therefore be

suitable for microwave radio applications while others will be favorable for use in satellite transmission.

For QPSK-, 8PSK- and 16QAM-based systems, the same block-coded Reed-Solomon code can be used. These codes only require hard decisions from the demodulator and provide the flexibility of a programmable code rate. Commercially available Reed-Solomon ASICs exist that can

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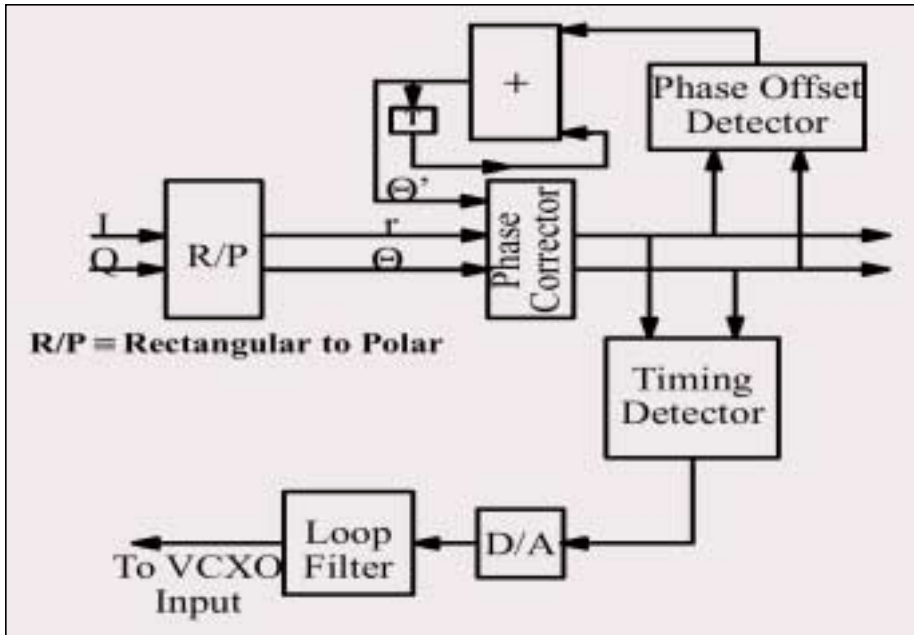


Figure 8. Architecture for carrier-phase synchronization and symbol-timing synchronizations.

handle as much as 300 Mb/sec.

Again, the control of such codecs is done using an FPGA. ACE schemes are simple to implement in hardware. The precoder and decoder required for ACE schemes are both of low complexity and can be implemented within an FPGA.

Design of higher data-rate systems models now allow for third-generation applications to higher data-rate transmission to be implemented.

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RF

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About the author

John Stannard was born and educated in Melbourne, Australia. He obtained his engineering qualifications from the Royal Melbourne Institute of Technology (RMIT), followed by extensive experience in the TV broadcast industry. His overseas experience involved study at Ryerson Institute Toronto while specializing in low-light image intensification for medical electronics with Westinghouse, (special products division) Baltimore as east coast service manager for the United States and Canada. He established JNS Electronic Industries in Australia, devoting 25 years to design and development of broadcast and telecommunications equipment with emphasis on RF transmission systems and the commercialization of spectrum-efficient microwave technology, the latter in conjunction with the University of South Australia. He is a commercial pilot with international experience. Stannard is a member of the IREE and IEA as a companion awarded for his endeavors to the telecommunications industry. He can be contacted at i61 3 9439 8257 (Australia), 61 3 9439 1000 (fax) or e-mail: jns@jns.com.au

Andrew Guidi and Phil McIlree were design and development engineers with the Institute for Telecommunications Research at the University of South Australia at the time this work was performed.