

Fast multitone analysis of RF transceivers

Full-chain simulations using harmonic balance and fast envelope techniques enable fast and full characterization of modern integrated radio transceiver ICs with thousands of transistors

By George Estep, Pete Johnson & Vladimir Veremey

RF design has changed, no doubt about it. Simply look at the fully integrated transceivers being designed today. RF design teams are faced with the challenge of integrating high-performance transceivers while still achieving low cost and low power. Unfortunately, the growing feature requirements and breadth of wireless standards have driven the complexity and sophistication of today's radios to new levels.

The demand for voice, high-speed data and even streaming video all jammed into the assigned spectrum makes the RF design challenge even greater. Cell phones and PDAs are planning to support as many as five different wireless standards within one handset. In fact, cell phone radio developers are actively putting multiple transceivers on the same chip to meet the demand for "wireless access anywhere." This frantic pace of integration is causing massive headaches among RF engineers.

In the midst of this feature and capability growth, RF designers are challenged to meet development deadlines, aggressive development costs and performance requirements. Picking a receiver or transmitter architecture to meet the various requirements can be a daunting task. A designer must weigh a staggering number of trade-offs to make these decisions. The high cost of spectrum, the increased need to transmit high bandwidth data and the cost pressures of the consumer market have forced designers to design better mixers, more efficient filters, higher amplifier sensitivities and a host of other improvements.

In a fully integrated transceiver, often the signal path contains a signal that is close to the carrier for down and/or up conversion, particularly with a low-IF or zero-IF architecture. Super-heterodyne architectures contain multiple mixers that must be analyzed in a multitone setting for proper linearity characterization. Additionally, simulating the small-signal noise and gain through the mixer in the presence of the large signal LO and a blocking signal is crucial to determine whether the

circuit will operate appropriately. Increasingly, modern radios contain complex, distributed and programmable gain-control schemes that allow linearity and noise performance to be fine tuned throughout the radio to achieve the best trade-off. Unfortunately, such schemes may require many thousands of analyses to determine the optimum circuit conditions for each signal and power level condition. There may be many different signals and power levels for which to tune the radio. These simulations cover the nominal design. The problem then increases many-fold as manufacturing variations are considered. Fast simulation and complex analysis are needed to gain confidence in the performance of the design prior to tape-out.

Harmonic balance for two-tone analysis

Traditionally, microwave integrated circuit (MIC) and monolithic microwave integrated circuit (MMIC) radios were simple enough, often comprising only tens of transistors. Hence, analyses could be easily performed at the transistor level. Today's integrated designs often contain thousands or tens of thousands of transistors and require many more separate simulations to be performed. Most radio architectures have one thing in common, a need to accurately and efficiently simulate multiple closely spaced tones on the entire transmit (TX) and/or receive (RX) chain. Harmonic balance is particularly well suited to this task because these

separate tones are independent. Time-domain techniques require a Nyquist sampling rate of twice the frequency of the highest frequency, typically the carrier, and must simulate long enough to cover the period of the lowest frequency, the difference between the two closely spaced tones until the transients disappear. This method is often inadequate due to the large number of time steps ($1/\text{Nyquist Frequency}$) needed. The simulation run-time required to cover a sufficient transient window for analysis is typically on the order of days. Many designers "work around" this limitation of time-domain tools by removing IF filtering and increasing the tone spacing. This approach carries both the risk of ignoring potentially significant effects of the filter and simulating the main circuit in a different band than it will be tested on the bench.

The ability to perform simulations on full TX and/or RX chains is fundamental to achieving a quality RFIC design that will meet performance expectations and yield well in high volume. Some harmonic balance simulators struggle with simulation capacity or maximum block size that can be successfully simulated. Historically, harmonic balance tools were used for board-level and microwave design and were not architected with today's capacity in mind. Legacy harmonic balance simulators require designers to break the design into small blocks for simulation and assemble the TX/RX simulation results manually. This cumbersome flow has led to accuracy problems and overall delays in de-

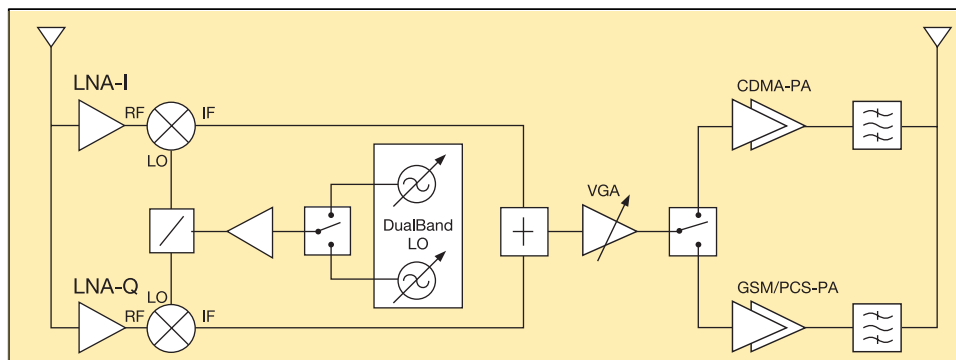


Figure 1. Dual-mode direct conversion transmitter (approximately 1200 transistors).

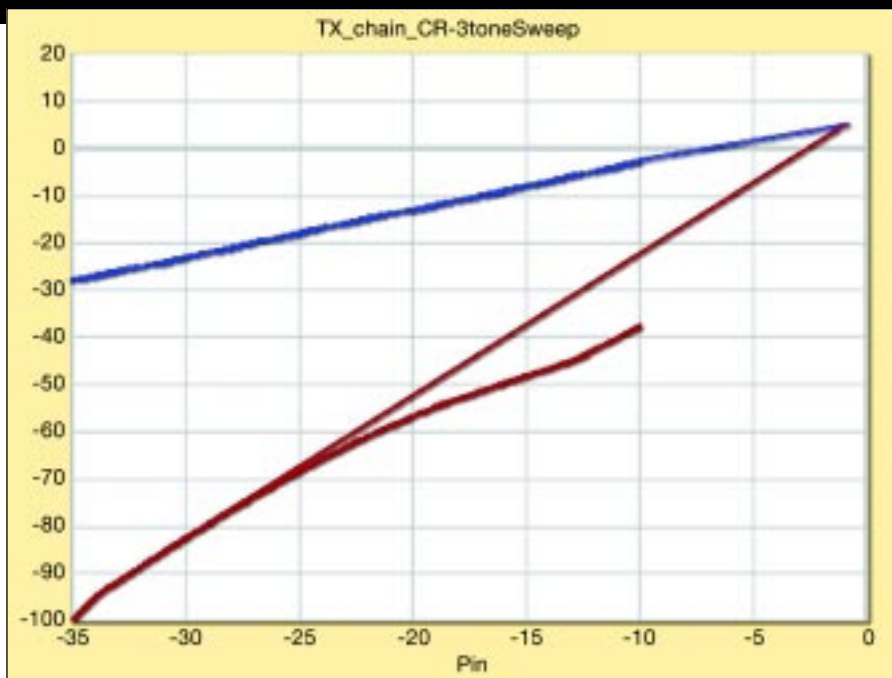


Figure 2. Simulation 1: Gain of TX chain for two-tone carrier analysis (harmonic balance) sweeping five point. Simulation run time is 5 mins, 3 seconds. Number of harmonics: 5 LO, 3 IF. development time.

Modern harmonic balance algorithms must be employed to handle the large number of active devices present in current RFIC designs. To run simulations on a full TX chain

often requires the simulator to converge on blocks greater than 3000 transistors. This number is expected to triple in the next year as even more complex transceivers enter the design process. A new generation of simula-

tion tools are now available that take advantage of efficient management of system memory, processing power and enhanced algorithms to enable the designer to converge on complete TX and/or RX chains quickly and accurately.

The following simulations were run on the transmitter chain illustrated in Figure 1. This transmitter is a reasonably complex design with roughly 1200 transistors. All simulations were run on a Linux PC with a 2.6 GHz processor and 1 Gbit of RAM. The simulation results are shown in Figures 2-4.

Layout and manufacturing effects

An additional trend that has been prevalent in radio design in recent years can best be described as a dearth of simulations to determine the effects of layout and manufacturing on radio performance. This has occurred almost solely as a result of long simulation times and capacity limitations. In many cases, designers do not feel they are adequately addressing the nominal case through simulation, so the idea of simulating circuits with extracted layout parasitics or performing 100 or 1000 Monte Carlo runs is somewhat ridiculous.

Harmonic balance, when it can be applied,

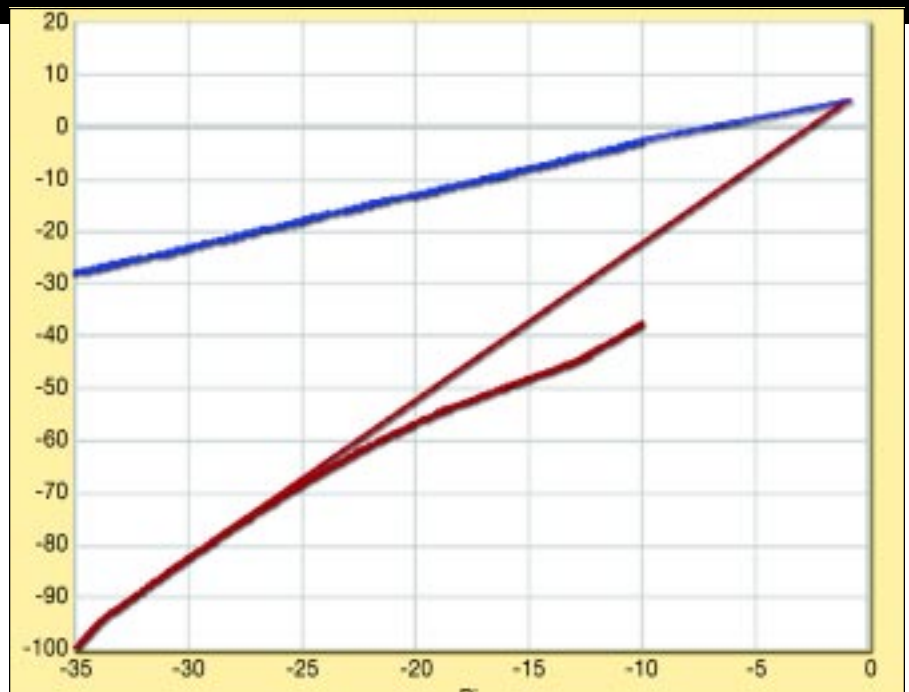


Figure 3. Simulation 2: IP3 for two tones sweeping nine power levels with tone separation of 10 MHz. Simulation run time is 39 mins,50 seconds. Number of harmonics: 4 LO, 3 IF, 3 IF. Memory used is 160 Mbytes.

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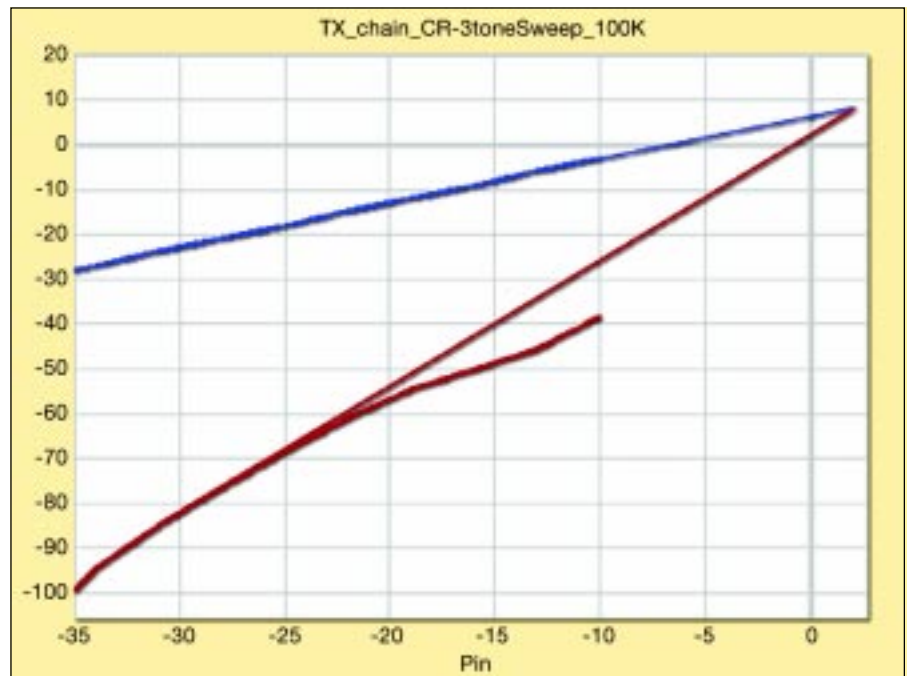


Figure 4. Simulation 3: IP3 for two tones sweeping nine power levels with tone separation of 100 kHz. Simulation run time is 37 mins, 10 seconds. Number of harmonics: 4 LO, 3 IF, 3 IF. Memory used is 160 Mbytes.

provides a significant benefit in these areas. Specifically, harmonic balance simulations do not bog down in the presence of large numbers of extracted layout parasitics in the way that time-domain approaches do. Often, simulations of this sort are only a couple times slower than their schematic-level counterparts.

In the area of simulating the effects of manufacturing variations, harmonic balance

really shines. This is due to the ability of harmonic balance to successfully use the solution from a previous run as a starting point for subsequent simulations. Often, subsequent runs can be performed in less than 1/10 the amount of time that was required for the initial solution. When combined with the earlier stated speedups for various multitone analyses, these improvements in Monte Carlo simulation can mean the difference between a

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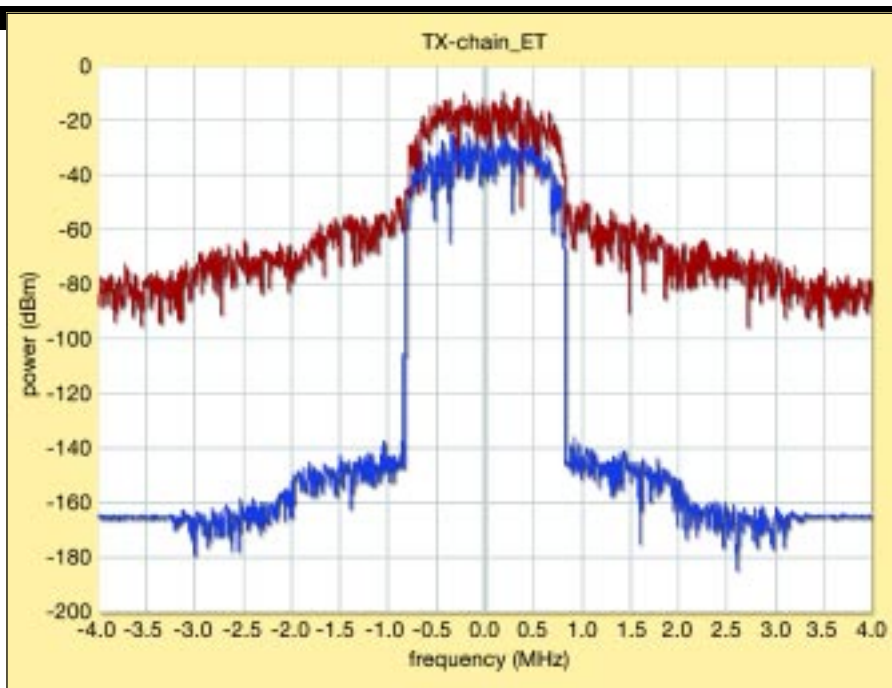


Figure 5. Simulation 4: Complete TX chain fast envelope transient simulation-band spectrum for IS95 signal, 128 bits QPSK source. Simulation run time is 12 mins, 26 seconds. Number of harmonics: 5 LO, 4 IF, 4 IF. Memory usage is 124 Mbytes.

design that is not fully characterized in the nominal condition and one that is fully understood over the process space.

Fast envelope transient analysis

As already demonstrated, harmonic balance simulation is effective for analyzing multiple tones in steady state. One limitation in using harmonic balance technique is the considerable increase in the number of state variables involved as the circuit becomes more non-linear or the number of non-linear devices in a circuit increase. Performing three-tone simulations on large structures eventually results in the memory-space limitations of modern 32-bit computers being exceeded.

As designers want to simulate real-world stimulus at the transistor level (IS95, WCDMA, etc.), Xpedion Design Systems has extended harmonic balance to properly handle modulated signals using fast envelope transient. This technique uses the benefits of steady-state sinusoidal analysis with the slow time-varying techniques of the modulating envelope to produce a superior solution to time domain or frequency domain alone. The approach also greatly reduces the memory required to perform multitone analysis compared to harmonic balance. This is done without sacrificing simulation speed. Indeed, for full-chain simulations, Xpedion's fast envelope analysis may be the only available solution for performing multitone simulations in a reasonable amount of time.

Furthermore, envelope transient technique is well suited for running simulations with real-world modulated sources. Using envelope simulation, one can analyze circuits with

input stimulus as RF carriers with time-varying complex envelopes such as amplitude and phase modulations. Their spectrum may represent transient signals or pseudo-random digital modulation with their continuous spectrum, or they may also include periodic signals with their discrete spectral lines, such as those representing the intermodulation products from a mixer or amplifier under multitone sinusoidal excitation.

Envelope transient technique handles the transient and steady-state analysis of RF circuits for arbitrary modulated carrier excitation, without excessive computational overhead. This technique considers a modulated signal as a combination of low-frequency dynamic (the envelope of the carrier or the modulation) and a high frequency dynamic (the carrier), which are analyzed separately and then merged together.

Envelope transient analysis predicts the response of a circuit when it is driven with a complex digital modulation signal. Interchannel interference resulting from intermodulation distortion is a critical analysis for digital wireless communications systems. Simple intermodulation tests involving only a small number of sinusoids as can be performed with harmonic balance are not a good indicator of how the non-linearity of the circuit couples the digitally modulated signals between adjacent channels. Instead, one has to apply the digital modulation, simulate with envelope transient and then determine how the modulation spectrum spreads into the adjacent channels. Envelope transient technique is useful in analyzing long-term behavior of certain RF circuits such as turn-on behavior of oscillators, power ampli-

fiers, turn-on and turn-off behavior of transmitters.

After using envelope transient simulation, a user at Cognio reported success in simulating a 5.2 GHz OFDM signal in a power amplifier and was able to extract ACPR. This simulation took about half an hour, which was significantly faster than expected. The Envelope design tool provides the ability to compute adjacent-channel power ratio (ACPR) and noise-power ratio (NPR) figures of merit, two of the most important design criteria for any power amplifier applied to any modern wireless system. It is also possible to directly visualize the impact of any amplifier design parameter on the ACPR and NPR. With Envelope transient one can quickly analyze the impact of complex modulations on each transistor's power dissipation and overall power consumption, which is not possible with classical system level design tools. Figure 5 demonstrates a complete TX chain simulation using Xpedion's GoldenGate simulator equipped with envelope transient analysis capability, an extension of harmonic balance. Design tools applying only harmonic balance techniques to calculate ACPR analysis are inaccurate because they first compute AM/AM/PM characteristics of the amplifier and then the quadrature phase shift keying (QPSK) signal on it. This does not provide any visibility to the internal operation of the power amplifier apart from the input and output characteristics with no information about power efficiency and harmonics. Also, such analysis results in inaccurate results for non-linear amplifiers or when the amplifier is driven into or close to its saturation point.

Conclusion

The ability to quickly perform full-chain simulations using harmonic balance and fast envelope techniques creates a new paradigm for RFIC development. Circuit simulation can move from a verification step in the design flow to an interactive design step. Complex simulations like multitone analyses that were often skipped can now effectively be used. Designers can tape-out designs with much higher confidence in the performance and manufacturability of the radio. Thus, RFIC simulators like Xpedion's GoldenGate have the capacity to converge on full TX and/or RX chains that are comprised of thousands of active devices and orders of magnitude in speed improvements. To ensure a fast learning curve and design portability, it is completely integrated with the Cadence Analog Design Environment. RFD

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