

# Designing military data-conversion systems involves multiple tradeoffs

A host of parameters including electrical, thermal, packaging, cost and reliability enter the mix when selecting data converter devices for high-performance military communications and radar systems.

By Mark Looney and Steve Reine

Converting RF signals to digital data that can be processed for a variety of system-level functions, analog-to-digital (ADC) and digital-to-analog converters (DAC) have enabled substantial leaps in the performance of advanced military/aerospace (mil/aero) communications and radar systems. Commercial ADCs and DACs are continually improving to meet the advancing needs of mil/aero systems, but the performance required by some of these systems continues to out-run commercial integrated circuit (IC) product development.

Mission-critical performance criteria can necessitate multiple conversion channels and more complicated system implementations. An example of a system that relies on continuous improvement in ADC capability and performance is synthetic aperture radar. In these systems, improved bandwidth yields greater azimuth and range resolution and improved noise/distortion performance yields greater receiver sensitivity.<sup>1</sup>

Development of these data conversion systems requires careful consideration of many parameters that represent a “data conversion trade space.” An example of the data conversion trade space can include critical performance such as sample rate, input bandwidth, resolution, dynamic range, noise, linearity, power dissipation, and support circuitry (analog front-end, clock drive, digital demux, etc.). In addition to electrical performance requirements, other factors such as package size/pin-out, thermal management, unit cost, project risk, component screening, and reliability can play a significant role in the development of data conversion systems.

The process of determining the appropriate integration path for military data conversion systems can require consideration of any subset of these criteria. Even though several integration options are available, system designers can feel constrained and may not fully understand the value of each option. Many times the pressure to use commercial-off-the-shelf (COTS) components can lead to more project risks and higher costs. In some cases, multichip modules (MCM) offer the best option. Other times, application-

specific integrated circuits (ASIC) are required to reduce unit cost and size or to create performance enhancements.

## Current conversion technology

The first step in the design of a system-level data conversion system will involve

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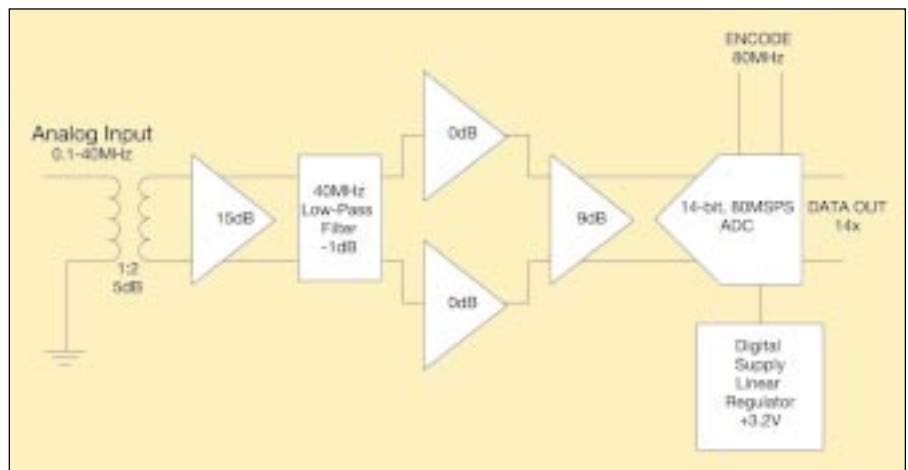


Figure 1. This 14-bit, 80-MSPS ADC MCM integrates many analog signal-processing functions for a mil/aero communications system.

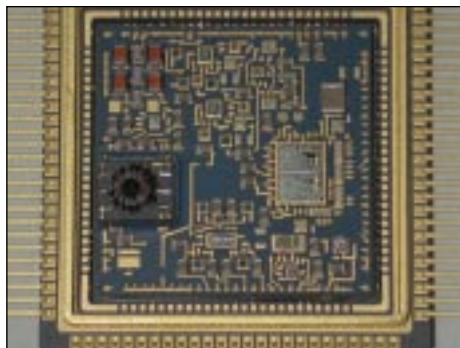


Figure 2. An internal view of the 14-bit 80-MSPS ADC MCM in Figure 1 shows a ceramic, hermetically sealed package that meets mil/aero environmental requirements.

determining exactly what is available in the COTS market. ADC/DAC IC products are usually designed to meet specific system requirements, but also to meet a broad range of requirements once they are released into mass production. The established performance of commercial components usually presents the least amount of risk, assuming that they provide the desired performance.

As an example, consider a new transmitter upgrade that requires a DAC with 12-bit intermodulation distortion (IMD) performance at analog frequencies up to 300 MHz, 14-bit resolution, and conversion rates greater than 1 GSPS. Low-voltage differential signaling (LVDS) 100 Ω

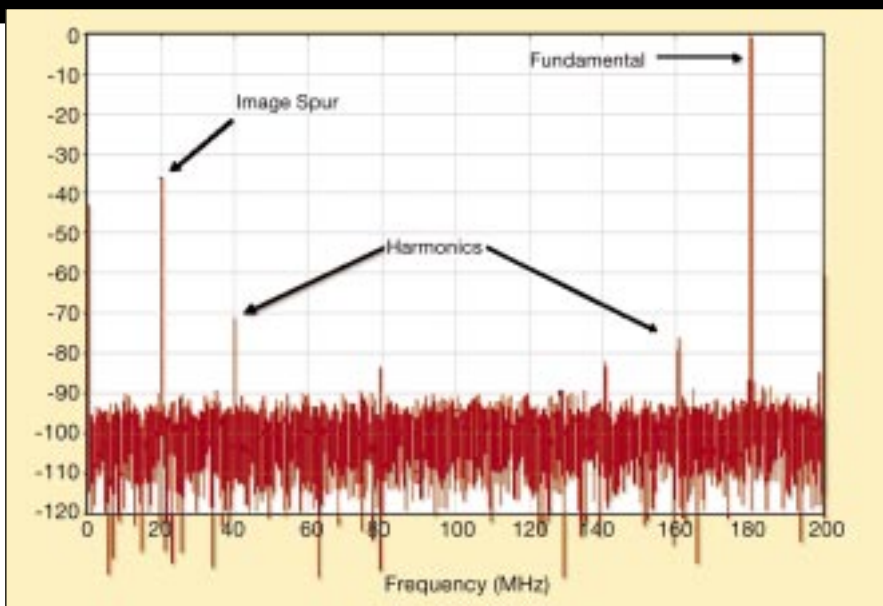


Figure 3. The FFT plot of a two-channel time-interleaved ADC shows the image spur resulting from gain and phase errors between channels in a two-channel system.

memory circuits are not fast enough to support these sample rates, so at least 2x interpolation will be required. Two power amplifiers having different input impedances are under consideration, creating the need for an adjustable output current. The system will be operated in remote locations, so the power dissipation must be less than 500 mW. Legacy system designs already use the serial peripheral interface (SPI) to program other devices, as well as 100  $\Omega$  LVDS digital circuits. Adherence to these standards will allow design resources to be allocated to higher-risk sections of the project. Another

piece of the design already presents a high level of risk, making the selection of a device that is designed on a commercial process technology (0.18 micron CMOS, for example) more attractive than an advanced process that has less demonstrated reliability.

In this example, the AD9736 14-bit, 1.2-GSPS DAC integrates all of the required features and performance in a single IC. But as advanced data conversion products enter the marketplace, system architects will still have to face several challenges to maintain these high levels of performance.<sup>2</sup> Achieving 74 dBc IMD and -158 dB/rt-Hz performance

at analog frequencies greater than 300 MHz requires careful consideration of clock drivers, layout, output matching, and isolation from many other threats to this performance. The data rate of 600 MHz (2x interpolation) requires fast memory and direct digital synthesis (DDS) functions. In some cases, integrating these functions into a MCM can reduce signal length runs, protect low-jitter clocks, improve filtering and provide other opportunities for adding value to system-level designs.

### MCM technology in mil/aero data conversion

MCMs have been used to implement packaging improvements in many mil/aero systems. Hermetic, ceramic MCMs offer size reduction, improved thermal dissipation, and reliability improvements for components that may be exposed to harsh conditions. In addition to these mechanical advantages, MCMs have also offered electrical performance advantages in military system designs. Performance improvements for data conversion MCMs can include increased gain, improved gain accuracy, extended bandwidth and reduced offset. Performance enhancements such as increased sample rates, improved distortion, and tighter power dissipation distribution can be obtained by screening conversion components at the component and MCM level, reducing the risk of yield loss at the system level. Finally, MCMs can be leveraged to create new functions that are not available in the form of single ICs.

For example, integrating a DAC function, such as the AD9736, with high-speed memory can be achieved with low risk and incremental cost increases. High-quality transformers and low-noise amplifiers (LNA) can be integrated with the best ADC functions in a single MCM package as well. This entire set of capabilities is available for mil/aero communications and radar system designers.<sup>3</sup>

It is important to note that while these capabilities exist, developing MCM solutions that rely on the availability of bare die can present substantial procurement challenges, as most semiconductor companies have either eliminated or severely restricted sales of bare dice. Thus, semiconductor companies require the presentation of appropriate business cases to justify providing products in this form factor. Many semiconductor companies have totally abandoned the MCM market, but some still actively evaluate opportunities to add value using this vehicle. This highlights the value in partnering with a semiconductor company that already provides all of the necessary IC components and is still active in serving the mil/aero market with MCM solutions.

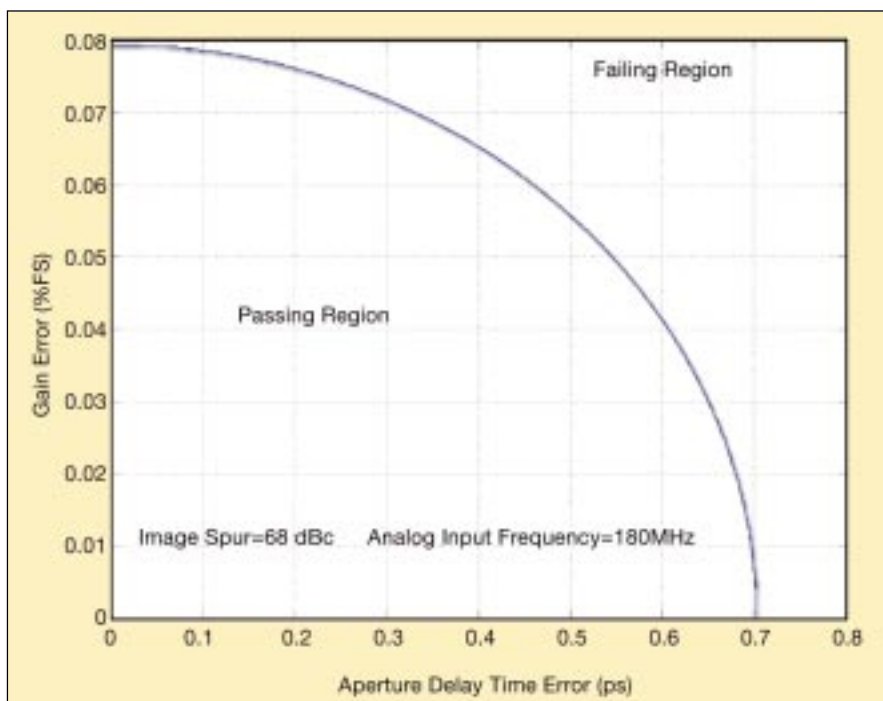


Figure 4. The error budget for a 180 MHz, 68 dBc time-interleaved ADC.

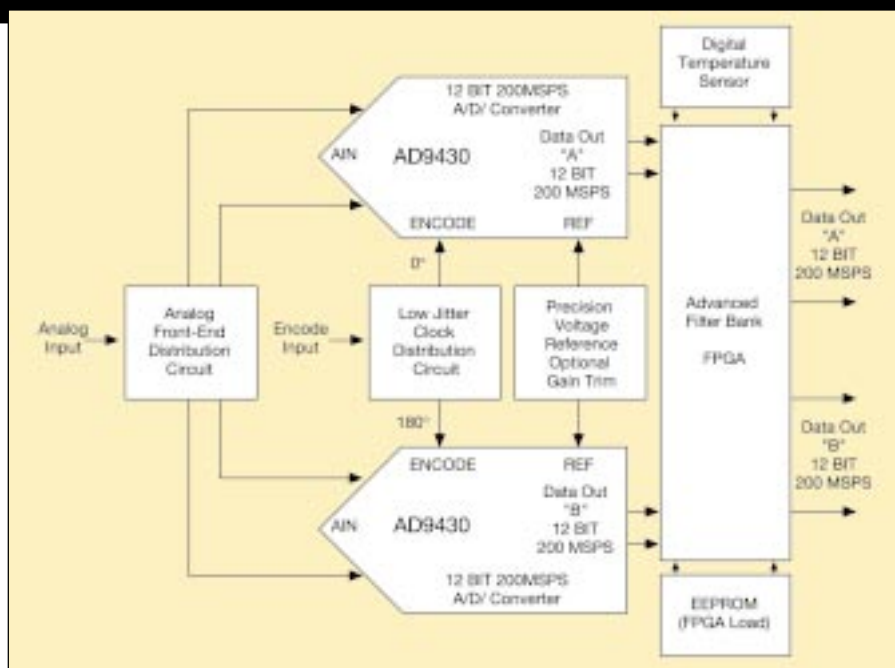


Figure 5. A two-channel time-interleaved MCM uses an advanced filter bank FPGA to provide digital channel matching for the two ADC channels.

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### Performance enhancement in an ADC MCM

The following example is an actual MCM developed for a mil/aero communications system. Integrating several important analog signal processing features along with a 14-bit, 80 MSPS ADC provided several benefits, which could be characterized in three basic areas: (1) enhanced performance and capability, (2) integration of multiple technologies in a single package, and (3) traditional mil/aero packaging benefits described in the previous section. The block diagram for this MCM is shown in Figure 1, and the internal view is displayed in Figure 2. It was packaged in a hermetic, ceramic gull-wing package that was designed for traditional mil/aero environmental conditions.

Performance improvements in this device included: increased sample rate (ADC up-screened from 65 MSPS to 80 MSPS), input signal gain of 28 dB while maintaining 65/80 dB SNR/SFDR performance, tighter gain/offset distribution with integrated trim networks, and a custom digital output voltage that reduces the risk of downstream damage to the system's processor. These benefits were achieved by integrating the following diverse technologies: ADC, amplifiers, power management components, discrete passive components, transformers and custom thin film networks. The sample-rate increase presented a substantial risk and

required the screening of wafer lots to identify appropriate material. This process would not normally be available for individual components. The integration of many components made this solution attractive for both system and component developers.

In addition to the obvious performance benefits, the final system benefited by having one of its most critical functions provided by a fully tested MCM rather than a collection of discrete components. The risk of system-level performance degradation due to marginal material was greatly reduced, and the quality assurance/reliability verification process was eased by qualifying a large number of components in a single MCM at one time.

Partnering with an appropriate MCM designer and manufacturer allowed this system development to benefit from reduced size, improved reliability, increased sample rate, larger front-end signal gain, noise/distortion performance maintenance, improved gain accuracy, and custom digital output voltages. The use of a chip-and-wire MCM packaging technology enabled the integration of multiple semiconductor process and passive component technologies into a single package, creating a single-component solution for this mil/aero data conversion requirement. Finally, this example illustrates the potential benefits when a semiconductor company that still serves the MCM market is presented with a design

challenge that also carries with it the appropriate business/market benefits. Without this level of partnership, this development would not likely take place.

### New function using MCM tech

The following example illustrates the use of MCMs in creating new system functions by leveraging time interleaving, a mature concept in high-speed ADCs.<sup>4</sup> This concept has been widely adopted in the test and measurement industry and has resulted in IC designs that are specific to these applications.<sup>5</sup>

To illustrate the concept of developing a new function using an MCM integration technique, consider a receiver upgrade that requires 12-bit resolution, a sampling rate of 400 MSPS, and at least 11-bit dynamic range at analog frequencies up to 180 MHz. At press time, the fastest commercially available 12-bit ADC was the AD9430, which is rated to run at 210 MSPS. Time interleaving would be a natural architecture to consider, but it presents an immediate threat to the 11-bit dynamic range performance (68 dBc). At a performance level of 10 bits and above, the most significant risk in this architecture is that the dynamic range is dependent on the gain, phase and offset matching between each individual ADC channel. Gain and phase errors between each channel generate distortion products known as image spurs, while offset errors generate distortion products known as offset spurs. Figure 3 provides an example Fast Fourier transform (FFT) plot from a typical two-channel time-interleaved ADC. Gain and phase errors generate image spurs that show up at  $fs/2 - A_{in}$  ( $A_{in}$  is the location of the analog input frequency in the first Nyquist zone). The offset spurs fall at the edge of the Nyquist band in the two-channel system, but become more of a problem for higher channel systems. In this two-channel example, the image spur falls into an area that reduces the available bandwidth to that of a single ADC.

This distortion product creates the need for high-precision correction techniques that hold their performance over wide bandwidths and temperature ranges. Figure 4 displays the gain/phase error budget associated with meeting a 68 dBc requirement at 180 MHz.

Achieving gain matching that is better than 0.1% and aperture matching better than 1 ps present a substantial challenge to any ADC system. While both analog and digital calibration techniques deserve consideration, the most likely solution will rely on digital techniques. The development of high-performance digital platforms and advanced digital post-processing techniques such as Advanced Filter Bank (AFB), from V-Corp Technologies present a unique opportunity for integrating the required channel matching

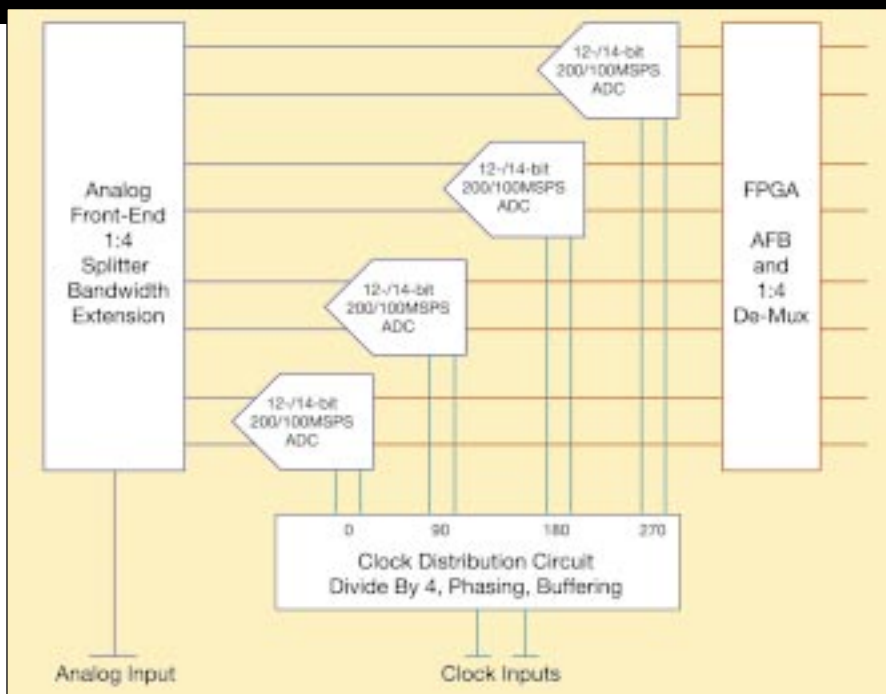


Figure 6. This 12-bit, 800 MSPS and 14-bit, 400 MSPS ADC is a four-channel ADC architecture that can serve as the foundation for future data conversion systems built around commercial ICs.

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function.<sup>6</sup> The level of performance provided by AFB is scalable—trading off processing power for calibration accuracy—to meet a variety of performance needs. A block diagram of a system that leverages this technology, along with all of its necessary support circuitry is shown in Figure 5. In this case, a field-programmable gate array (FPGA) was used to implement the digital post-processing algorithm.

The clock distribution circuit, precision voltage reference, power management and single-ended-to-differential transformer front-end circuits are included in this diagram. Instead of requiring a central clock to generate two 200 MHz signals that are precisely 180° out of phase from one another, the local clock circuit handles that function, requiring only a single 400 MHz input signal from the system’s clock generation circuit. Considering the tight stability/matching requirements on the clock distribution circuit, integrating this function in close proximity to the ADCs can be critical. Device selection, tight layouts and thermal matching are common analog techniques that can be used to reduce the processing burden on the digital post-processing hardware. Integrating common reference and power distribution circuits provides

similar advantages—reducing the risk associated with known threats to the tight matching requirements. The analog front-end circuit provides two primary benefits: single-ended analog inputs and the ability to “tune” the analog input bandwidth of the ADCs.

An example of integrating the block diagram into an MCM can be found in the AD12400 12-bit, 400 MSPS ADC that incorporates the AFB technology and provides system designers with an integrated solution not available in commercial ICs.<sup>7</sup> This MCM-based technology represents more than just an advancement of an old idea; it represents a new paradigm of integrating multiple technologies (SiGe clock driver circuits, high-quality data conversion, power management, and advanced digital signal processing hardware/techniques) into a single data conversion solution.<sup>8</sup>

### Toward the future

Even as the data conversion market continues to experience the development of advanced performance capabilities in ICs such as the AD9736, MCM technology will continue to offer value in its ability to integrate diverse technologies and reduce risk.

Future mixed-signal MCMs will offer additional functionality through the integration of the best LNA and ADC technologies. They could also offer added functionality by integrating DDS/RAM capabilities with cutting-edge DAC technologies.

The next level of integration in the time-interleaving technology will include four-channel architectures such as the one displayed in Figure 6. These architectures will provide mil/aero system design engineers with 12-bit/800 MSPS and 14-bit/400 MSPS ADC functions using ICs that are commercially available.

The development of this architecture will involve the consideration of multiple integration paths. A building block integration approach could offer the three main functions of clock, ADC, and digital post processing as separate modules that form a chip set. This approach provides standard, functional blocks that can be made available for other multichannel ADC system architectures and that offer a simple path for digital upgrades.

Another approach would integrate all of the functions in Figure 5 except the digital hardware into a single MCM. This would provide tighter location of critical components that are sensitive to thermal, power supply, mechanical, and other environmental conditions. The presumption in this case would be that the closer proximity reduces the risk to environmentally caused channel matching errors while still providing a path for simple digital hardware upgrades.

As data conversion technology continues to advance, these integration decisions will continue to be critical in mil/aero systems that seek to maximize the performance advantage of each technology advance. **DE**

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