

# Quantifying system performance of GSM/GPRS PAs with differing levels of integration

The two key power amplifier metrics are power and efficiency. When comparing power amps with different levels of integration, the context of how the specifications are defined is important. The performance of the system solution is referenced to the antenna and battery, then distilled into one metric.

By Mendy Ouzillou

As little as three years ago, GSM power amplifier (PA) solutions were poorly integrated. The transmit system solution required individual ICs for low-band, high-band and power control and many discrete components for input and output matching networks, harmonic filtering, decoupling capacitors and all the support components for the power control function. This lack of integration was due to process technology, simulation tools, requirement for high-Q (low-loss) passives, and stringent requirements of the 3GPP (GSM) specification. However, in the last two years, PA solutions have integrated external functions and components into a multichip module, thereby decreasing the footprint and the complexity of the solution. Most recently, PA technology advanced even further with the availability of a monolithic solution that further reduces the bill of materials and design complexity.

Measuring and comparing PA performance is no simple matter for design engineers. Key metrics used to quantify PA performance have been redefined due to improvements in integration. To compare PAs with different

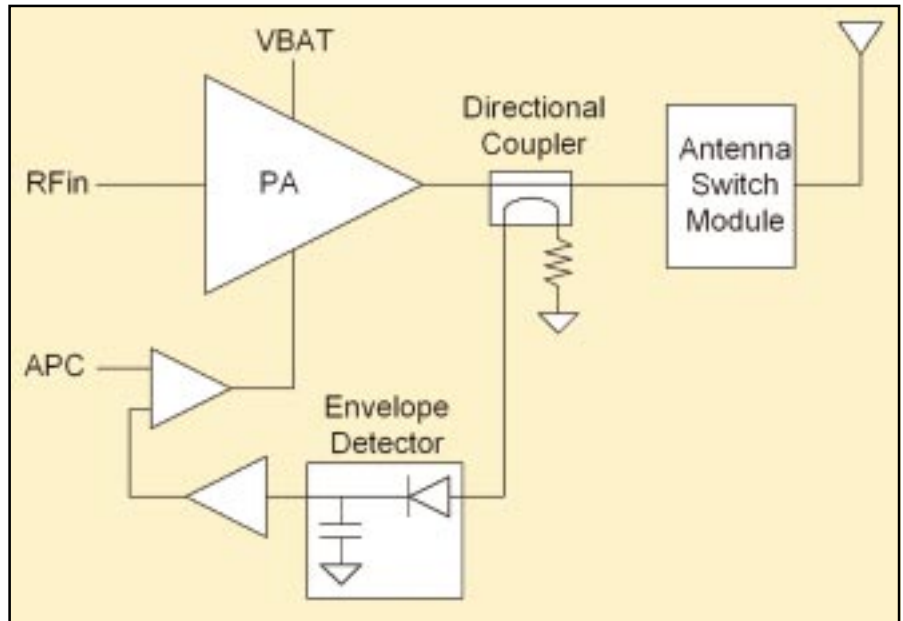


Figure 1. Closed loop power control architecture.

levels of integration, the context of how the specifications are defined is as important as

the specification itself. To enable an effective comparison of two PAs with differing levels of integration, the performance of the system solution will be referenced to the antenna and battery and then distilled into one metric: average burst current. With minor modifications, these concepts can be extended to benefit any RF transmit system.

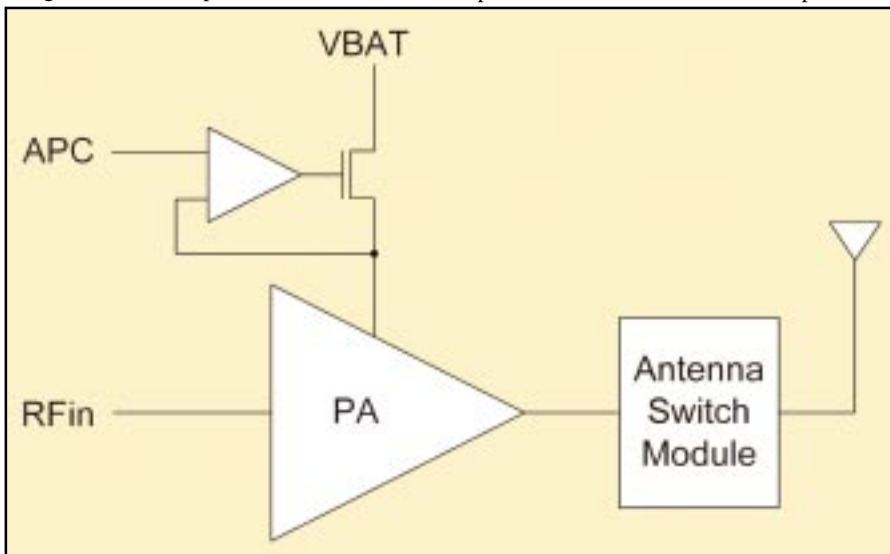


Figure 2. Supply voltage power control architecture.

## PA output power vs. power at the antenna

The best way to evaluate PAs with differing levels of integration or architectures is to specify the power requirements at the antenna and work back to the requirements for the PA. The typical calibrated power level at the antenna (according to industry norms) is 32.75 dBm for low-band (GSM) and 29.75 dBm in high-band (DCS).

The power control architecture used in the transmit system will impact the amount of power the PA needs to generate in order to meet the requirements at the antenna. Closed-loop, supply voltage and supply current power

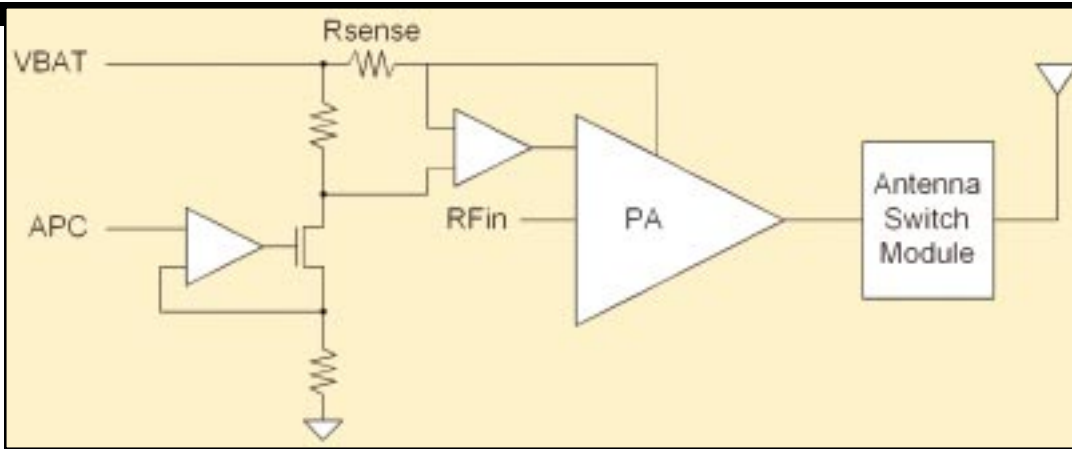


Figure 3. Supply current power control architecture.

Power at antenna (GSM)	Monolithic PA	External Closed-Loop Power Control PA
PA maximum output power (dBm)	34.2	35.0
PA efficiency at max power	50%	52%
Resistive losses ( $\Omega$ ) between battery and PA	0.12	0.12
Voltage present at the PA battery input (V) after losses	3.52	3.49
PA output power loss due to new operating voltage (dB)	0.00	0.00
Insertion loss due to directional coupler, harmonic filter and any loss between PA and ASM (dB)	0.00	0.45
Insertion loss due to antenna switch module (dB)	1.20	1.20
<b>Power required at the antenna</b>	<b>32.75</b>	<b>32.75</b>
<b>Operating power of PA (dBm)</b>	<b>33.95</b>	<b>34.40</b>

Table 1. PA operating power based on power at antenna.

control (Figures 1-3) are the most widely used power control architectures.

Recent multichip module (MCM) and monolithic solutions that completely integrate power control can be treated as a black box allowing the system designer to only worry about the output power level. However, in less integrated solutions, the type of power control will impact output power requirements.

The closed-loop power control architecture was the most commonly accepted form of power control. Some popular PA solutions still use external power control and incur the insertion loss associated with the external directional coupler. The PA must generate an additional  $\sim 0.25$  dB for GSM and  $\sim 0.30$  dB for DCS to compensate for the additional insertion loss.

The supply voltage power control architecture has gained wide acceptance partially due to not requiring the use of a directional coupler. This power control architecture requires a large MOSFET or regulator between the PA and the battery. The monolithic power amplifier solution uses supply voltage power control and integrates the regulator. Though most solutions using this type of power control have integrated the entire power control circuitry, some PA solutions still require an external MOSFET device. The external MOSFET inserts  $20\text{ m}\Omega$  to

$100\text{ m}\Omega$  of resistance in series with the battery that reduces efficiency and lowers output power. The lower output power is a consequence of voltage drop that occurs during a burst across the series resistance between the battery and PA. This voltage drop lowers the operating voltage of the PA and thus lowers the output power.

The final power control architecture controls the output power by sensing the current

PA Efficiency 50.00%		
Insertion Loss After PA (dB)	System Efficiency	Delta in Efficiency
0.10	48.86%	1.14%
0.2	47.75%	2.25%
0.30	46.66%	3.34%
0.40	45.60%	4.40%
0.50	44.56%	5.44%
1.00	39.72%	10.28%
1.10	38.81%	11.19%
1.20	37.93%	12.07%
1.30	37.07%	12.93%
1.40	36.22%	13.78%
1.50	35.40%	14.60%
1.60	34.59%	15.41%
1.70	33.80%	16.20%

Table 2. System efficiency degradation due to insertion loss.

flowing in the battery line to the PA. The sense resistor is typically  $75\text{ m}\Omega$  to  $100\text{ m}\Omega$ . This resistance between the battery and the PA will reduce efficiency and potentially reduce output power. Due to its complexity, most solutions that use this type of power control integrate all required elements including the sense resistor.

Many solutions available today have marginal harmonic performance and the system engineer must evaluate the impact of additional filtering on the output power requirements. If the system requires additional harmonic filtering beyond that offered by the ASM, then the PA will have to provide an additional  $0.20$  dB of power to compensate for insertion loss.

By examining the key issues affecting output power, one can compare the output power required from two PA solutions with differing levels of integration.

### System efficiency vs. PA efficiency

The 3GPP specification does not mandate any specific efficiency for the mobile station (MS); however, the most "efficient" MS will have the longest talk time. Though the PA has a tremendous impact on talk time, it is not necessarily true that the PA with the highest efficiency will lead to the longest talk time.

Fundamentally, system efficiency corresponds to the current supplied by the battery in order to achieve a specified output power level at the antenna. Therefore, it is important to comprehend all resistive losses along

PA Efficiency 30.00%		
Insertion Loss After PA (dB)	System Efficiency	Delta in Efficiency
0.10	29.32%	0.68%
0.20	28.65%	1.35%
0.30	28.00%	2.00%
0.40	27.36%	2.64%
0.50	26.74%	3.26%
1.00	23.83%	6.17%
1.10	23.29%	6.71%
1.20	22.76%	7.24%
1.30	22.24%	7.76%
1.40	21.73%	8.27%
1.50	21.24%	8.76%
1.60	20.75%	9.25%
1.70	20.28%	9.72%

PA Output Power (dBm, W)	34.20	2.63		
PA Efficiency	50%			
DC power during burst (W)	5.26	(at PA battery terminal)		
Battery Voltage (V)	3.70			
Resistive Loss ( $\Omega$ )	Battery Current (A)	Voltage at PA Battery Terminal	System Efficiency	Delta in Efficiency
0.100	1.48	3.55	48.00%	2.00%
0.150	1.51	3.47	46.93%	3.07%
0.200	1.55	3.39	45.81%	4.19%
0.250	1.59	3.30	44.62%	5.38%

**Table 3. System efficiency degradation due to resistive loss.**

PA Output Power (dBm, W)	34.20	2.63		
PA Efficiency	50%			
DC power during burst (W)	5.26	(at PA battery terminal)		
Battery Voltage (V)	3.70			
Loss Mechanism	Current (mA)	Efficiency	Delta in Efficiency	
Current difference in competing transceiver solutions	87.00	47.12%	2.88%	
Secondary power supply	7.00	49.76%	0.24%	
Closed-loop power control circuits + APC current	8.00	49.72%	0.28%	

**Table 4. System efficiency degradation due to miscellaneous currents.**

the DC path from the battery to the PA, insertion losses between the PA and the antenna switch, the PA and system operating conditions and any additional current consumption from external and internal circuits. Understanding these loss mechanisms will reveal the system efficiency and the PA's

impact on that system efficiency.

Small losses between the PA and antenna can have a significant impact on the system efficiency. As Table 2 illustrates, the impact on system efficiency is not correlated to the PA's output power but to the PA efficiency at that output power and the losses following the PA.

Due to the impact on efficiency, there is a strong drive to minimize the insertion loss of all the components between the antenna and the PA, especially the antenna switch module (ASM), which has the highest insertion loss. The goal is not just to reduce insertion loss and thus use a lower output power PA, but also to use a PA with the lowest possible output power whose efficiency has been optimized for that lower power.

As seen in Table 3, any resistive losses in the path between the battery and the PA will degrade system efficiency. In this case, the impact on efficiency is directly proportional to the PA's output power level.

The system designer can reap big benefits from minimizing the resistance between the battery and the PA for example, by making sure that the battery connector is close to the PA.

A more subtle aspect of system efficiency requires evaluating miscellaneous currents from secondary power supplies and external support circuitry. Additionally, transceiver currents should also be included to capture the drive power required from the transceiver to the PA input.

Having listed the significant loss terms, the definition of PA efficiency can be expanded to include all the loss terms and thus become system efficiency. System efficiency will then enable a first order comparison between any two PAs.

By adjusting the power of the PA to produce the same power at the antenna for both PAs, the system efficiency numbers stated above offer an excellent metric of system performance. Note that in Table 5, the starting PA efficiency of the external closed-loop power control PA is higher but the system efficiency is lower after factoring in all the losses.

### Average burst current

Deriving the system efficiency and output power requirements for the two PAs enables the calculation of the current drain on the battery, the average burst current (ABC). ABC enables the designer to incorporate the two important figures of merit, system efficiency and power at the antenna, and combine them into one value that takes into account the entire transmit system. No other metric can so easily and succinctly distill such a complicated issue as power amplifier efficiency and output power.

The average burst current is defined as the burst current averaged across the bursts:

$$ABC = (\text{output power at antenna}) / (\text{system efficiency} \times \text{battery voltage})$$

The ABC can be easily converted into talk time by using the following conversion:

$$\text{Talk time} = \text{Battery Capacity} \times 8 / ABC$$

System designers face difficult design

System Efficiency	Monolithic PA	External Closed-Loop Power Control PA
PA efficiency at max power	50%	52%
Operating power of PA (dBm)	33.95	34.40
Adjusted efficiency based on operating power of PA	48%	48%
Resistive losses ( $\Omega$ ) between battery and PA	0.12	0.12
Voltage present at the PA battery input (V) after losses	3.52	3.50
System efficiency loss due to resistive loss	2.29%	2.55%
PA efficiency loss due to new operating voltage	0.00%	0.00%
Efficiency loss due to directional coupler, harmonic filter and any loss between PA and ASM (dB)	0.00%	4.72%
Efficiency loss due to antenna switch module.	11.59%	11.59%
Miscellaneous currents (mA)	82	82
Efficiency loss due to misc. currents	2.66%	2.41%
<b>System Efficiency (efficiency at antenna)</b>	<b>32.8%</b>	<b>29.6%</b>

Table 5. Comparing system efficiencies of two different PAs.

Power Amplifier (GSM)	Power at Antenna (dBm)	Efficiency at Antenna	Average Burst Current (mA)
Monolithic PA	32.75	32.8%	1550.1
External Closed-Loop Power Control PA	32.75	29.6%	1719.8

Table 6. Comparison of two PAs based on ABC.

challenges throughout the entire development process. Like any other project, the task of comparing and selecting components can seem daunting when there are so many choices, especially when those choices offer

varying degrees of integration. When choosing between PAs, it is important to redefine the meaning of the key parameters based on the context of integration. Average burst current enables system designers

to make the decision based on the more real world comparison of system performance.

(Note: This article assumes an antenna load of 50  $\Omega$  for GSM900 and DCS1800 and nominal PA operating conditions of 3.5 V and 25° C. The battery operating voltage is 3.7 V. The calculations presented in the spreadsheets can be found online at [www.silabs.com/pa-calculations](http://www.silabs.com/pa-calculations).) RFD

#### ABOUT THE AUTHOR

Mendy Ouzillou serves as marketing manager for Silicon Laboratories' GSM/GPRS power amplifier product line. Ouzillou joined Austin, Tx.-based Silicon Laboratories in 1999 and has also managed key segments of the company's RF synthesizer product family. With 15 years experience, Ouzillou has held design engineering and management positions with National Instruments and Applied Research Laboratories (ARL). Ouzillou holds a bachelor's degree in electrical engineering from the University of Texas at Austin.