

Low-power receiver architecture for interference-robust UWB radio

Ultra-wideband wireless communications promises unprecedented levels of seamless connectivity between consumer electronics devices, enabling gigabytes of data to be transmitted in seconds rather than hours without exhausting the batteries of hand-held portable devices. To meet the low-cost requirement of consumer product applications, the multiband-orthogonal frequency-division multiplexing (MB-OFDM) system has been designed to minimize transceiver architecture complexity.

By Domine M.W. Leenaerts and Jozef R.M. Bergervoet

Ultra-wideband (UWB) wireless communication promises unprecedented levels of seamless connectivity between consumer electronics devices, enabling gigabytes of data to be transmitted in seconds rather than hours without exhausting the batteries of hand-held portable devices such as digital cameras, audio jukeboxes and mobile phones. The FCC has opened up spectrum in the 3.1 GHz to 10.6 GHz range for unlicensed UWB operation, and the WiMedia Alliance (an amalgamation of the WiMedia and Multiband OFDM Alliance SIG groups) is proposing transmission standards that will encourage worldwide acceptance of UWB by accommodating anticipated differences in spectrum allocation from regulatory bodies around the world.

The alliance's main standard, known as MB-OFDM (multiband-orthogonal frequency-division multiplexing) transmits data simultaneously over multiple, accurately spaced, carrier frequencies and features high spectral flexibility plus resilience to RF interference and multipath effects. To meet the low-cost requirement of consumer product applications, the MB-OFDM system is designed to minimize transceiver architecture complexity, requiring a single analog receive chain, relatively low-resolution ADCs and DACs and limited internal precision in the digital baseband.

It divides the allocated spectrum into several QPSK-OFDM (quadrature phase shift keying-orthogonal frequency-division multiplexing) modulated sub-bands, spaced 528 MHz apart, and employs a frequency-hopping scheme between these sub-bands to achieve efficient and robust communication for piconets operating simultaneously in close proximity. Transmit power remains below the FCC limit of -41.25 dBm/MHz, and frequency hops take place every 312.5 ns.

Implementing the receiver chain is not, however, without challenges. The low RF signal level requires the use of a low-noise receive chain, while the potential presence

of strong out-of-band interferers in the 2.4 GHz and 5 GHz bands (for example, Bluetooth and IEEE 802.11a/b/g links) requires a receiver with high linearity and

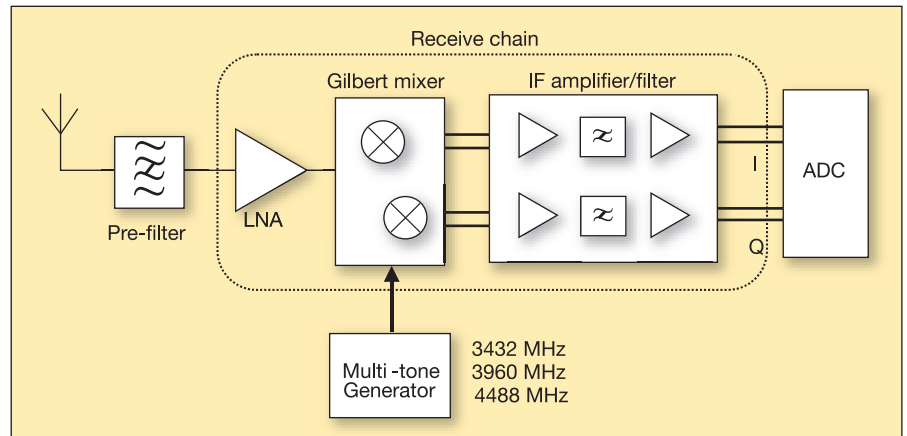


Figure 1. Philips' UWB receive-chain architecture.

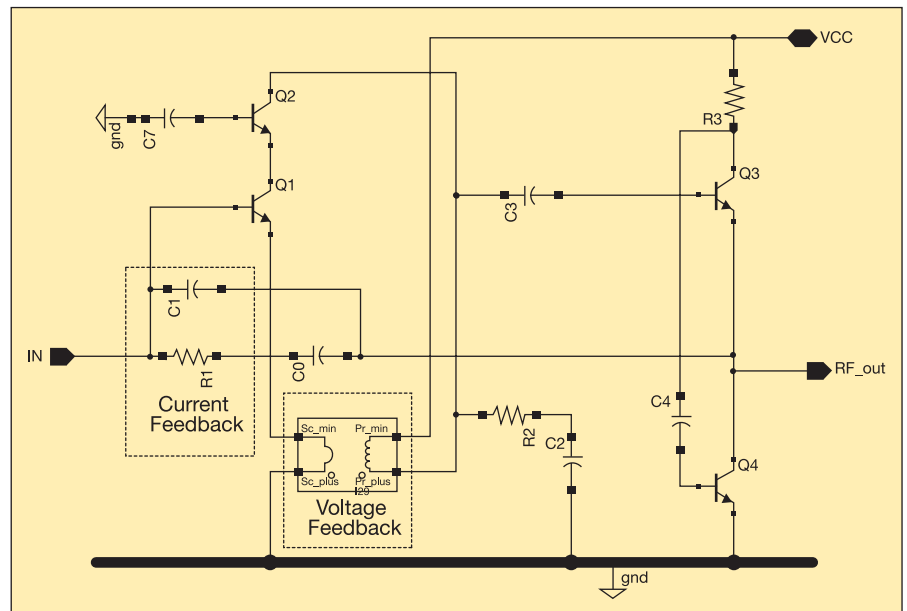


Figure 2. Voltage and current feedback loops in the LNA correct linearity in the absence of balanced differential inputs.

selectivity. The transceiver must be able to hop between carrier frequencies within 9 ns, and the carriers generated by its frequency synthesizer must be spectrally pure. For example, spurious tones in the 5 GHz range must be below -50 dBc to avoid downconversion of strong out-of-band interferers into wanted signal bands.

The receiver must be able to discriminate the wanted UWB signal, which may be as weak as -70 dBm at a distance of 10 meters from the transmitter, in the presence of a nearby interferer such as an 802.11a transmitter from which the received signal level is around +23 dBm and whose frequency is only 500 MHz away from the UWB carrier. This poses challenges in the design of the receiver front-end over a very wide bandwidth with respect to noise and distortion. Furthermore, to limit the dynamic range in the subsequent ADCs, the interferer has to be filtered to a level well below the wanted signal, requiring a wide-band IF filter with high attenuation and an accurate and steep roll-off.

RF architecture

To meet these requirements, a receive-chain architecture as illustrated in Figure 1 was developed. It was test-chip implemented in a new QUBiC4G silicon-germanium BiCMOS process technology. QUBiC4G realizes the high transistor f_t figures required for operation in the 3.1 GHz to 10.6 GHz band and also features the passive component integration capabilities required to create a highly integrated solution.

The radio is based on a zero-IF architecture with the frequency hopping realized in a multitone frequency synthesizer. An off-chip pre-filter reduces strong out-of-band interferers. The single-ended low-noise amplifier (LNA) input avoids the added complexity of an external wideband balun, thereby minimizing RF signal loss and system cost. Generation of true differential signals is left until the Gilbert mixer stage, where it is achieved through the use of an active balun under-stage. The Gilbert mixer generates quadrature (I and Q) outputs, which are filtered and amplified by the IF filter amplifier, after which they are digitized in separate ADCs.

Although the single-ended LNA configuration significantly reduces system cost (no external wideband balun required), it slightly worsens input linearity. Linearity is corrected by applying voltage and current feedback to the LNA, as shown in Figure 2. This feedback matches the input impedance to 50 Ω over the lower three MB-OFDM sub-bands in which this receiver chain is designed to operate (3432 MHz, 3960 MHz, and 4488 MHz), without the need for external amplifying components.

The I and Q local oscillator inputs for the

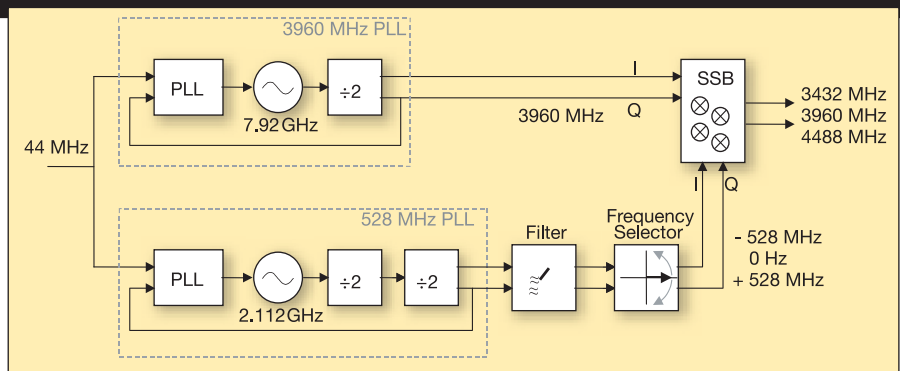


Figure 3. Block diagram of the multitone frequency synthesizer.

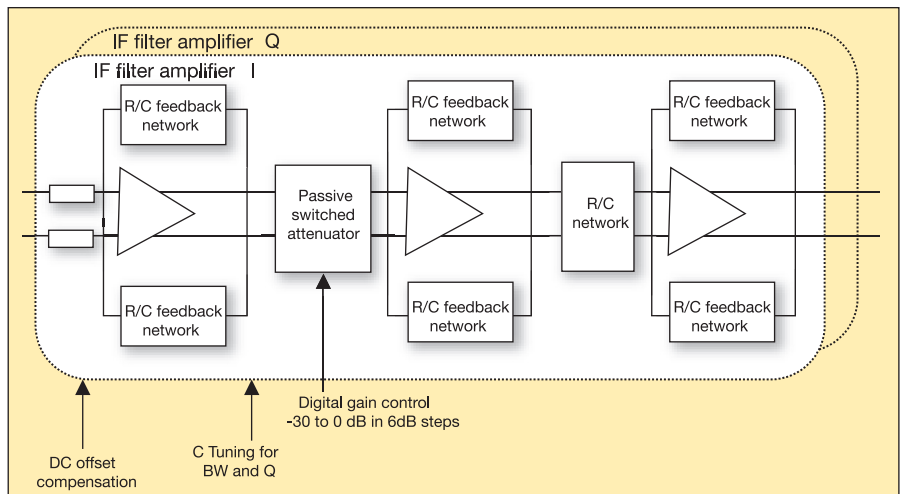


Figure 4. IF filter architecture.

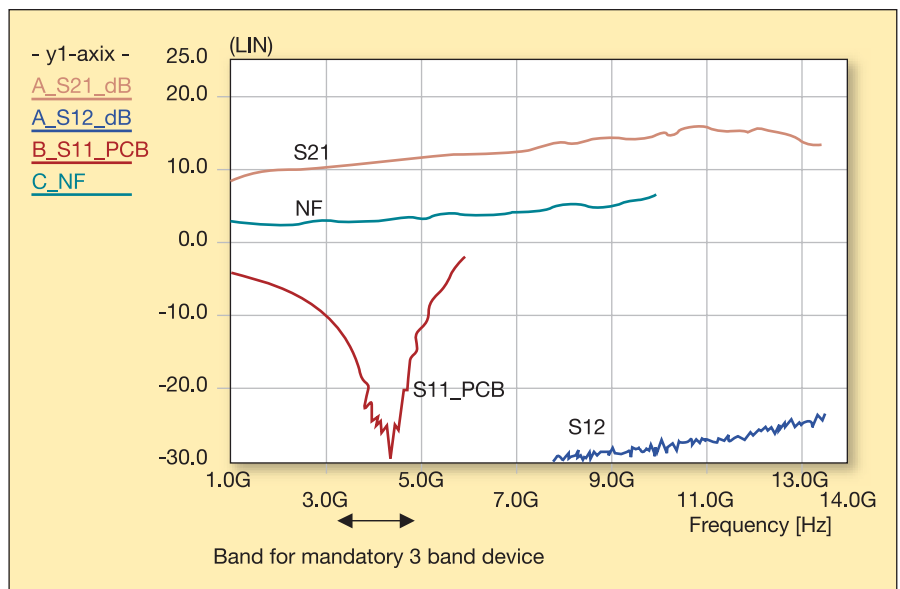


Figure 5. LNA frequency response curves in dB for gain (S21), noise figure (NF), return loss measured on pcb (S11_PCB) and reverse isolation (S12).

Gilbert mixer are generated by a multitone frequency synthesizer, which has also been test-chip fabricated in Philip's QUBiC4G silicon germanium (SiGe) process technology. There are a number of ways of generating the three local oscillator frequencies for the sub-bands, obvious options being the use of a single fast-settling phase-locked loop (PLL)

or three separate PLLs feeding a three-way RF switch. However, the first of these would require an unrealistically high reference frequency to achieve the required settling speed, while the second solution would be sensitive to inductive coupling between the three PLLs and to carrier leakage between them.

The chosen architecture for the frequency

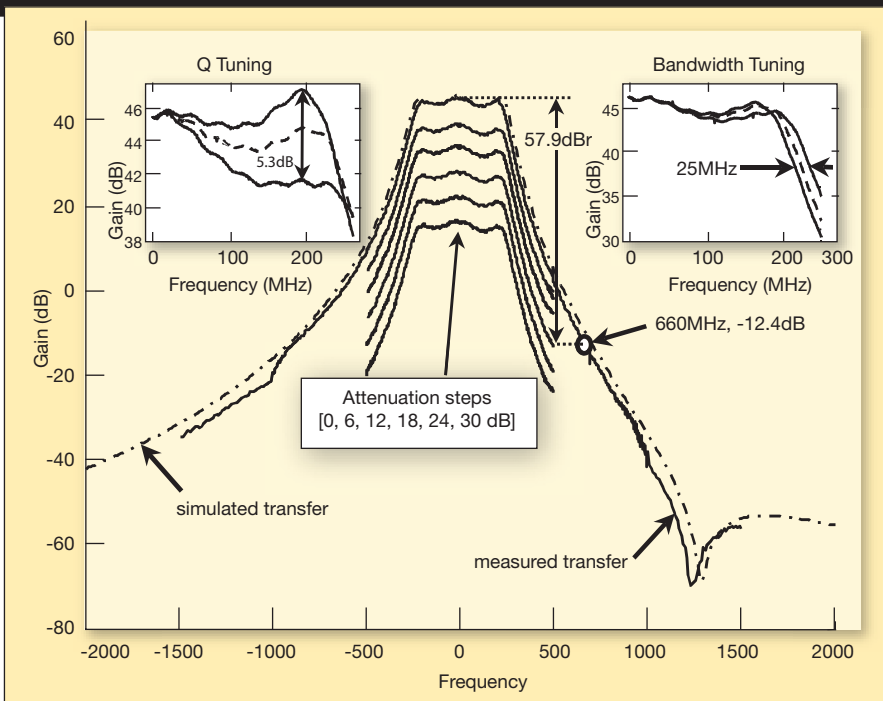


Figure 6. Transfer characteristics of the IF filter.

synthesizer uses two quadrature I and Q PLLs, one generating a local oscillator frequency for the middle sub-band (3960 MHz) while the other generates a frequency equal to the sub-band spacing (528 MHz). The upper and

lower sub-band local oscillator frequencies are then generated by mixing the outputs of these two PLLs in a single-sideband (SSB) mixer, inverting the sign of the 528 MHz frequency to generate the upper and lower sub-band

carriers (3960 MHz + 528 MHz = 4488 MHz and 3960 MHz – 528 MHz = 3432 MHz). The 3960 MHz signal is simply shifted by 0 Hz to generate the local oscillator frequency for the middle sub-band. Using this architecture, the achievable frequency hopping speed is well below 1 ns.

A block diagram of this multitone generator is shown in Figure 3. The filter is needed to suppress the third harmonic that is generated in the 528 MHz PLL’s frequency divider, which could otherwise result in in-band spurious signals being generated after downconversion in the presence of a strong interferer such as an 802.11a signal. Both local oscillators use inductors to minimize phase noise and power dissipation and are tuned by digitally controlled MOS capacitors, all of these components being integrated on-chip using the passive integration capabilities of QUBiC4G process technology.

After mixing the RF input with the local oscillator signals in the Gilbert mixer, the quadrature IF frequency outputs are filtered in a fully differential low-pass Chebyshev active filter with a nominal gain of 45 dB and a passband ripple of 2.8 dB. This filter comprises multiple gain stages, filter stages and passive switched attenuators (Figure 4) that are distributed in a way that makes the IF chain highly linear, both when the wanted signal is weak and strong interferers are present, and when the wanted signal level is high. The filter also provides a high level of rejection to large out-of-band interferers, which receive only limited attenuation ahead of the LNA. The better the IF filtering, the closer the receiver can co-exist with local interferers such as 802.11 wireless networks. One of the most severe situations is an 802.11a interferer at 5.15 GHz, which is only 660 MHz away from the carrier frequency of the 4488-MHz UWB sub-band.

To achieve the transition-band and stop-band accuracy, the position and quality factor of the filter poles is digitally calibrated by switched-capacitor arrays realized using high capacitance density (5 fF/μm²) metal-insulator-metal (MIM) capacitors that are integrated on-chip as part of the QUBiC4G BiCMOS process technology. These capacitors are used to calibrate out process-induced variations in performance. The nominal tuning range of the band edge is 25 MHz in 16 steps. The high f_t figures (>70 GHz) of the transistors in the QUBiC4G process provide the filter’s two-stage differential amplifiers with the high unity-gain frequency needed to maintain low distortion levels. The attenuator is a digitally switched passive resistor network and achieves an attenuation range of 0 dB to –30 dB in steps of –6 dB.

Performance results

Measurement results for the naked die

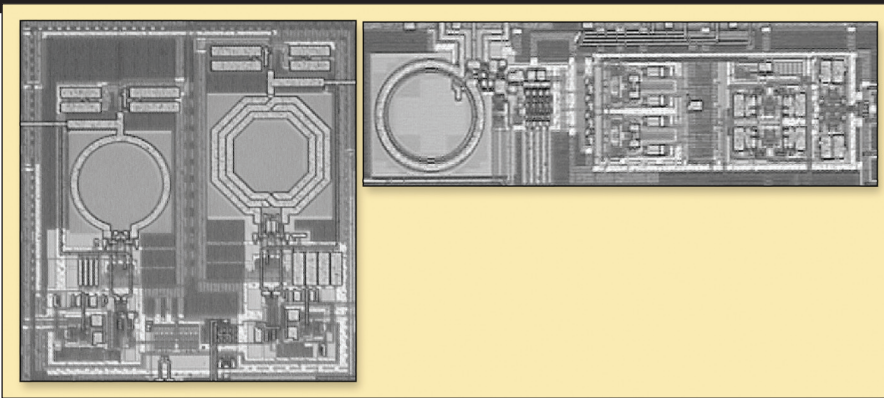


Figure 7. Micrographs of the multitone synthesizer (left) and LNA/mixer/IF filter (right) clearly show the passive component integration capabilities of Philips' QUBiC4G RF BiCMOS process technology.

LNA are shown in Figure 5. Excellent gain and noise figures are maintained up to around 13 GHz, making this receive-chain design suitable for the full 3.1 GHz to 10.6 GHz UWB frequency range. Input impedance matching was measured with the die mounted in a HVQFN package assembled onto an FR4 laminate printed circuit board, because both the device package and the board mounting affect the impedance match. These test results, therefore, represent typical application conditions. Figure 6 shows the measured magnitude transfer characteristics of the IF filter for different gain and bandwidth settings. The gain can be varied between 16 dB and 46 dB in 6 dB steps, and the bandwidth can be tuned in the range 232 MHz to 254 MHz. At 660 MHz offset a -57 dB_r was achieved.

Phase noise tests on the multitone frequency synthesizer operating in the 4488 MHz UWB sub-band show in-band phase noise to be below -90 dBc/Hz and out-of-band phase noise to be below -100 dBc/Hz at 1 MHz offset. The signal-to-noise ratio over a single UWB channel is, therefore, degraded by less than 0.1 dB as a result of phase noise in the multitone frequency synthesizer. When operating in the same sub-band, spurious tones in the 5 GHz band are below -50 dBc. With a realistic antenna filter, a worst-case $+23$ dBm 802.11a interferer at 20 cm distance will be attenuated by 20 dB, sufficient to avoid a severe interference problem. A similar reasoning holds for the 2.4 GHz ISM band where the requirement is set to -45 dBc. The measured spurious tone at 2.37 GHz is attenuated by -46 dBc and sufficiently suppressed to allow coexistence between UWB and 2.4 GHz ISM users.

The complete prototyped receiver draws less than 80 mA from a 2.7 V supply (approximately 47 mA for the receive-chain and 27 mA for the multitone frequency synthesizer). Micrographs of the two test-chips are shown in Figure 7.

When developing a receive-chain architecture for UWB operation in the 3.1 GHz to 10.6 GHz bands, a designer must meet certain requirements. Passive component integration capabilities are required to create a highly integrated solution. **RFD**

ABOUT THE AUTHORS

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