



PLL frequency synthesizer handles 8 GHz

To simplify system design and cut costs in high-frequency wireless systems, **Analog Devices** has developed an integrated 8 GHz phase-locked loop (PLL) frequency synthesizer that eliminates the need for frequency doublers. Designed for wireless systems, such as those used for broadband wireless access, satellite communications, instrumentation, wireless LANs and base stations for wireless radio, the new ADF4108 is the highest-frequency PLL synthesizer currently available on the market, according to the manufacturer. The device can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters.

It consists of a low-noise digital phase frequency detector (PFD), a precision charge pump, a programmable reference divider, programmable A (6 bit) and B (13 bit) counters, and a dual-modulus prescaler (P/P +1). The A and B counters, in conjunction with the dual-modulus prescaler, implement an N divider ($N = BP+A$). In addition, the 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. The ADF4108 has a power supply range of 3.2 V to 3.6 V and a separate charge pump supply (VP) allows extended tuning voltage in 3.3 V systems. A complete PLL can be implemented if the synthesizer is used with an external loop filter and voltage-controlled oscillator (VCO). Operating temperature range for the device is -40°C to $+85^{\circ}\text{C}$.

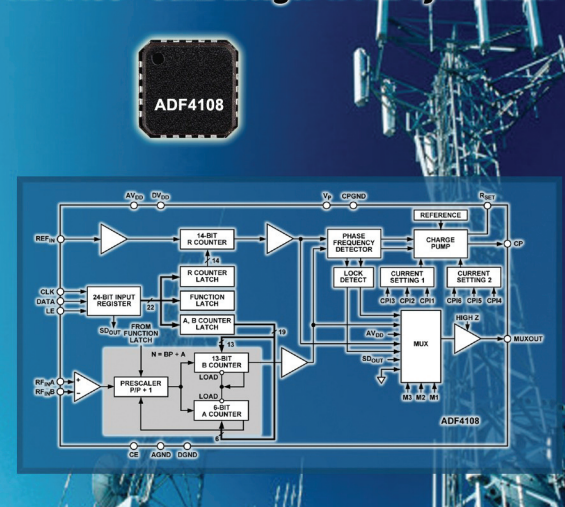
Other features include a three-wire serial interface to control on-chip registers, hardware and software power-down mode, and loop filter design with ADIsimPLL. In fact, the manufacturer recently upgraded ADIsimPLL to version 3.0. The improved simulator offers a comprehensive PLL design and simulation package for ADI's range of PLL frequency synthesizers, enabling rapid prototype development and design optimization. ADIsimPLL version 3.0 is available free of charge as a download from ADI's web site, thereby allowing designers to run simulations locally.

Normalized phase noise floor of the PLL synthesizer is given at -219 dBc/Hz (typical). Hence, the phase noise performance of ADF4108 at 7.9 GHz is rated at -81 dBc/Hz (typ.) at 1 kHz offset and 1 MHz PFD. Implemented in $0.35\text{ }\mu\text{m}$ BiCMOS process, the ADF4108 is pin compatible with 6 GHz PLL synthesizer ADF4106. Power consumption is 60 mW.

It is available in a lead-frame chip-scale package (LFCSP) and is priced at \$3.30 per unit in quantities of 1,000.

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ADF4108 - 8GHz Integer-N PLL Synthesizer



PLL frequency synthesizer's 8 MHz bandwidth eliminates the need for frequency doublers in many high frequency systems, simplifying system architecture and reducing cost.