

Alternative approach to a low-cost wideband amplifier

By Geoff Stokes

An alternative approach to the development of a wideband amplifier should take into account the effect of its package and its printed circuit interconnections for accurate analysis of high-frequency and microwave circuits. In this analysis, we have departed from a lumped-element model based on quasi-static approaches, which do not take accurate account of RF current and field distributions in complicated structures, such as package pins and printed circuits containing plated via holes. The objective can then be deduced: If reiteration is to be minimized, the simulation results must match the measured results as accurately as possible. In practice, there are always departures, but each step taken to narrow the gap will yield a benefit.

The device was designed primarily for the intermediate frequency (IF) channel of a domestic satellite TV receiver. The low noise block (LNB) collects the satellite signal at about 12 GHz using a dish antenna. The LNB amplifies and downconverts this RF signal to an IF of about 1 GHz to 2 GHz. This is done because it is too expensive to guide the collected RF signal directly to the TV receiver in the living area. To solve this problem, the dish assembly includes a bracketed housing containing an RF low-noise amplifier and frequency converter. Also in the housing are IF amplifiers that drive the down-feed cable. The module on the bracket is known as an LNB. Special requirements exist for the external antenna-mounted circuits:

- Low-cost, small die in plastic package.
- Low power dissipation.
- Moderately low noise and distortion.
- Wide operating temperature range.
- Good stability margin.
- Broadband match to 50 Ω or 75 Ω .

The low-cost requirement has affected the choice of technology. A silicon bipolar process was adjusted to achieve bandwidth with suitable noise figure (NF) and non-linear distortion. This and other aspects of the process were optimized as a compromise between a number of transistor parameters including third-order intercept (IP3). The simulation included extensive substrate coupling analysis so that the overall RF circuit performance was optimized. The package effect was also included as previously mentioned. This allows optimization of overall circuit behavior.

A photograph of a two-layer printed circuit for test purposes is shown in Figure 1, and the schematic is in Figure 2. The top



Figure 1. Amplifier test circuit board.

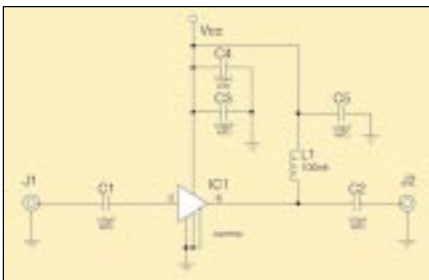


Figure 2. Test circuit schematic.

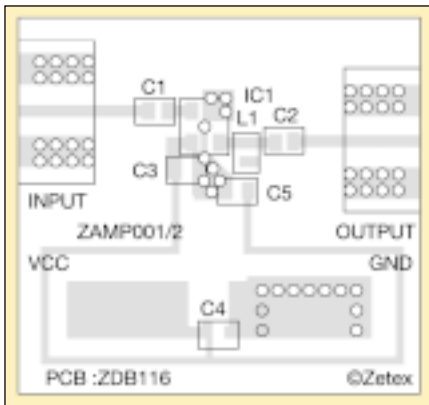


Figure 3. Printed board layout.

copper layout is shown in Figure 3, showing the positions of via holes, which are 0.5 mm in diameter and the silk screen component identifications. The board thickness is 0.4 mm with a continuous copper ground plane on the bottom. Near the amplifier, IC1, the via holes are placed closely to minimize the return current paths to ground, yet the effect of these vias is significant and needs to be accounted in the analysis.

For the broadband application, the package requires more attention compared to a narrowband case. The broadband circuit demands optimization of parameters over the frequency range, including impedance match to 50 Ω , gain and isolation. In the narrowband case, once the chip design has been finalized, the application circuit can be optimized using

tuned matching circuits on the printed circuit board. These matching circuits compensate in part for the distributed parasitic reactance of the package and its immediate printed circuit environment, including printed microstrip or strip-lines and plated-through via holes. Some literature mentions “via inductance” as a separate entity. Where the copper surface current changes direction, for example, from horizontal stripline current to the vertical via, the electromagnetic fields in the dielectric are somewhat complicated and are related to a similarly complicated surface current. This will be further involved by the tendency of trace currents to become radial near the end of the via. This may be seen as a superposition of various wave modes. Therefore, if short sections of track and vias are treated separately, there will be errors in calculations of equivalent lumped circuit values as an approximation to the distributed inductance and capacitance.

To include such distributed effects as much as possible, the package was analyzed using a full-wave electromagnetic simulator, including the printed circuit copper immediately local to the device, and the all-important ground vias that complete the microstrip connections. The full-wave nature of this analysis includes the multiple modes around the vias as mentioned earlier.

The full-wave simulator chosen was CST Microwave Studio. This provides a full-wave linear circuit description with S-parameter output in Touchstone format. This file can interface directly to Cadence to be incorporated within the overall circuit simulation. Together, with the substrate coupling mentioned earlier, the simulation includes most of the distributed circuit effects. In this way, the distributed effects both on and off the chip were included in the full circuit simulation, which could then be further optimized for detailed parameter requirements for the temperature and frequency ranges including gain, return losses, NF, IP3, stability and power consumption. RFD

ABOUT THE AUTHOR

Geoff Stokes is a systems engineer at Zetex Semiconductors plc, Oldham, UK. He has a physics degree from Oxford University, UK (1972) and is a chartered engineer (MIEE). He has worked on analog and RF circuit and system development.