

# Accelerating the design and verification process

Several factors must be taken into consideration when creating a signal in simulation and downloading the simulated signal to an RF signal generator's arbitrary waveform (Arb) generator.

By Greg Jue

One of the primary applications for combining EDA with test solutions is to create real-world RF test signals from the EDA simulation. This capability allows the flexibility of design simulation to create arbitrary RF signals with such design impairments as fading and multipath present in the RF test signal. Two considerations in supporting a signal flow from EDA to a signal source generator include: (1) carrier frequency and modulation bandwidth and (2) the number of IQ data pair samples required for the application.

To support this general capability, the signal generator must be able to accept data created from an EDA simulation and turn it into a real RF test signal. Typically, this simulation data would be in the form of IQ data pairs as a function of time or samples, as shown in Figure 1.

The IQ data pairs created from simulation and downloaded to the signal source are then modulated onto an IF/RF/microwave carrier using the IQ modulator in the signal generator to turn the simulated signal into an actual test signal. Depending on the application, it may be useful to turn the simulated signal into an IF/RF/microwave test signal or a digital test signal.

## Carrier frequency and modulation bandwidth

The IQ modulator in the signal generator must have the modulation bandwidth to support the signal format being generated in simulation, where the simulation bandwidth is defined by the simulation time step to be used to sample the I and Q envelopes:  $\text{Simulation Bandwidth} = 1 / (\text{Time step})$ , where Time step is the time step used to sample  $I(t)$  and  $Q(t)$  to construct the real RF signal  $S(t) = I(t) \cdot \cos(2\pi Fc t) - Q(t) \cdot \sin(2\pi Fc t)$ .

Note that the time step is used to effec-

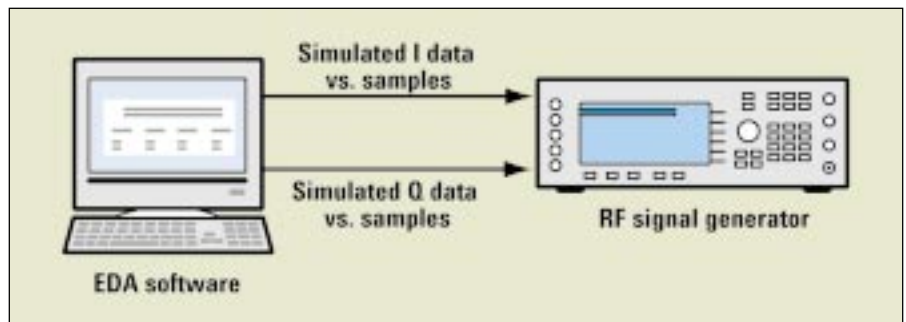


Figure 1. Turning a simulated signal into a real RF test signal.

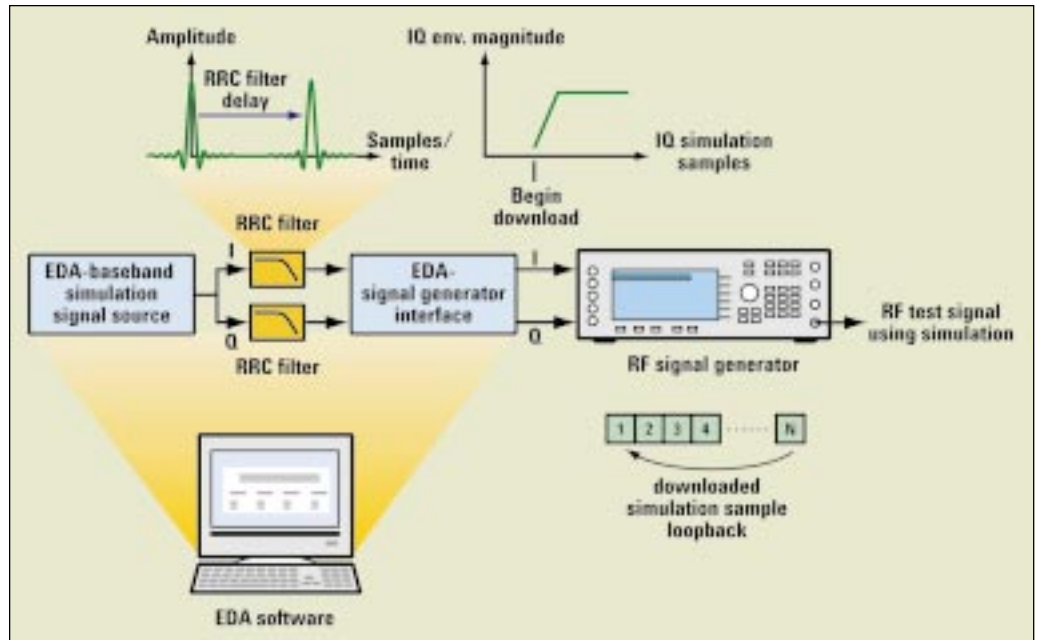


Figure 2. Considerations in setting the simulation start sample to download to the signal generator.

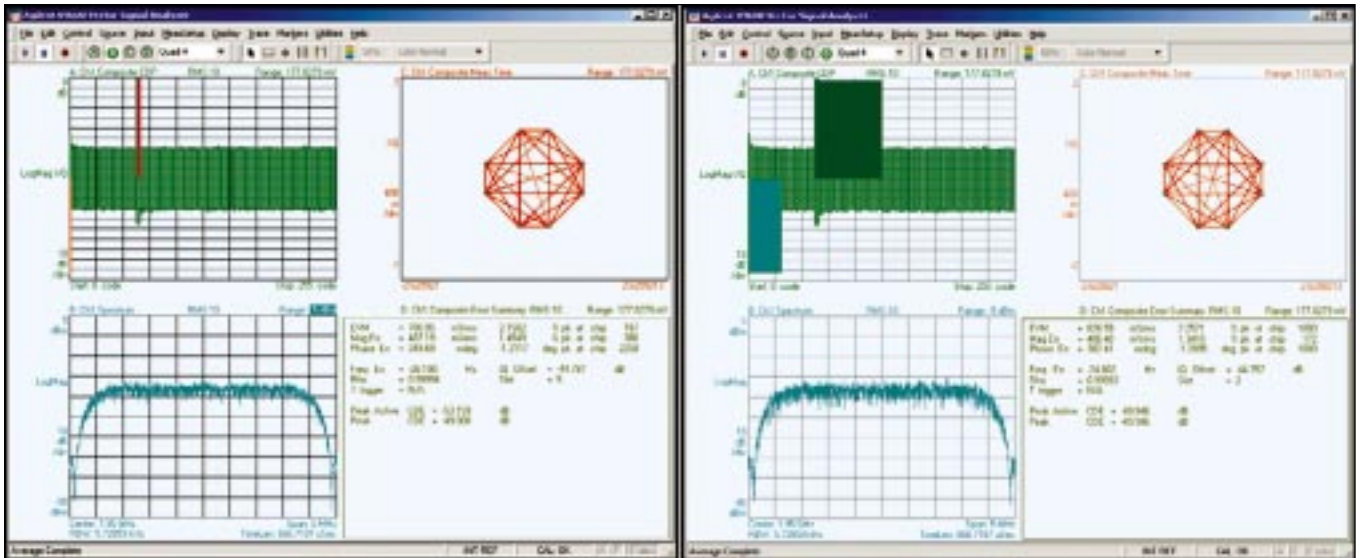
tively sample the I and Q envelopes and not the carrier frequency itself.

Typically, the signal generator would allow a finite number of simulation samples to be downloaded and stored within the signal generator. It is, therefore, important to consider setting the start sample for the simulation data being downloaded to account for any delays in the simulated design (such as delays from Root Raised Cosine (RRC)

filters) so that the first sample downloaded corresponds to the start of the frame as shown in Figure 2.

Note that  $N$  number of simulation samples are downloaded from the EDA software to the signal generator arbitrary waveform generator (Arb). Typically, the  $N$  simulation samples would then be repeated in a loopback mode in the RF signal generator, where the simulation data record is repeated when the

*For signal formats with a coded frame structure, this can be addressed by ensuring that the first sample of data downloaded from the EDA software corresponds to the beginning of a frame, and the total number of simulation samples downloaded corresponds to an integer number of frames.*



**Figure 3. Correct (left) vs. incorrect (right) EDA-to-RF signal generator interface configuration.**

last simulation sample has been played. If the first and last sample are not carefully considered or well-conditioned, this loopback mode can result in discontinuities between the last sample and first sample as they are looped back, which in turn, could degrade waveform quality, performance, and spectral dynamic range. For signal formats with a coded frame structure, this can be addressed by ensuring that the first sample of data downloaded from the EDA software corresponds to the beginning of a frame, and the total number of simulation samples downloaded corresponds to an integer number of frames.

For example, the calculations for downloading 15 frames of WCDMA data are shown below, assuming a simulation signal source filtered by an RRC filter with an alpha of 0.22, which is then downloaded to a signal generator (Figure 2).

### WCDMA example

- RRC filter length = 16 chips long, equivalent to a 64-tap FIR at four samples/chip.
- Download 15 frames with optimal waveform quality.

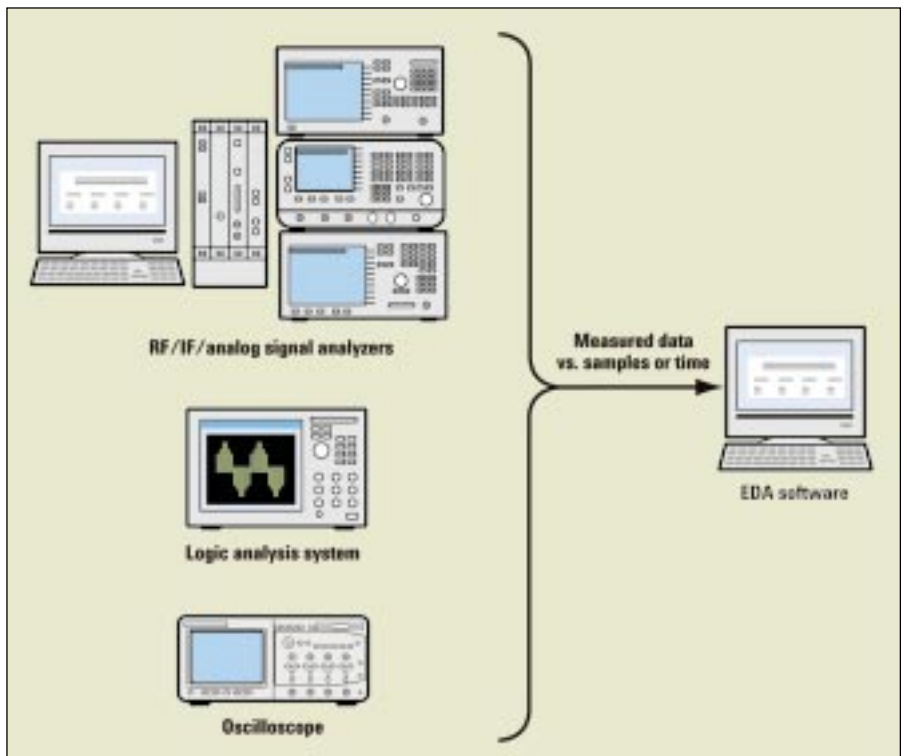
The delay through this RRC filter can be calculated as:  $(16 \text{ chips}/2) * 4 \text{ samples/chip} = 32$  simulation samples from the equation shown in Figure 2. In terms of time, this would translate to 32 simulation samples /  $(4 * 3.84 \text{ MHz})$  or 2.08333 microseconds ( $\mu\text{s}$ ) given the simulation time step.

The number of samples to be downloaded for 15 frames of data can be calculated as:  $15 \text{ frames} * 15 \text{ timeslots/frame} * 2560 \text{ chips/}$

$\text{timeslot} * 4 \text{ samples/chip} = 2,304,000 \text{ samples}$ . This corresponds to  $15 \text{ frames} * 10 \text{ ms/frame}$  or 150 ms of data.

Thus, the first simulation sample that should be downloaded from the EDA solution to the RF signal generator is sample

number 32, and the last sample to be downloaded is sample number 2,304,032 (start sample +2,304,000 samples for 15 frames). This should help mitigate any “wraparound” discontinuity effects and provide optimal waveform quality.



**Figure 4. Different types of signal analyzers to capture measured data for EDA simulation.**

Figure 3 shows two signal analyzer displays where the start and stop sample have been carefully considered (left), vs. a case where the start sample being downloaded to the RF signal generator has not been carefully considered (right). The simulation was set up to reflect the calculation above for the left plot. The start sample was set to zero for the right plot, not taking the RRC filter delay into account. Each plot was measured with 10 averages. Although a constellation is shown for the right plot, it was intermittent as the VSA lost and reacquired carrier lock. Note that the composite code domain (CDP) power does not clearly discern the orthogonal variable spread factor (OVSF) codes from the EDA solution on the right plot. Also, a minimum of one frame (or 15 time slots) is required for the VSA to demodulate with its default measurement result length, or no measurement results would be displayed.

### IQ data pairs

The maximum number of IQ data pairs that can be downloaded from the EDA simulation to the signal generator can also be an important consideration, particularly for receiver bit error rate (BER) or packet error rate (PER) applications. For example, BER/PER measurements typically require downloading enough data from the EDA simulation to the signal generator to measure a statistically meaningful BER or PER result. The number of data bits required for the BER/PER measurement translates to a number of required IQ data pairs to be downloaded from the EDA solution to the signal generator. Considerations include: (1) the coding structure of the signal format; (2) the sampling rate needed for sufficient waveform quality; and (3) the number of frames/bits that must be measured to achieve a statistically meaningful result or to meet a given specification. A given Arb memory depth may be sufficient for BER/PER measurements for one signal format, but perhaps not for a different signal format as a result of the considerations mentioned above.

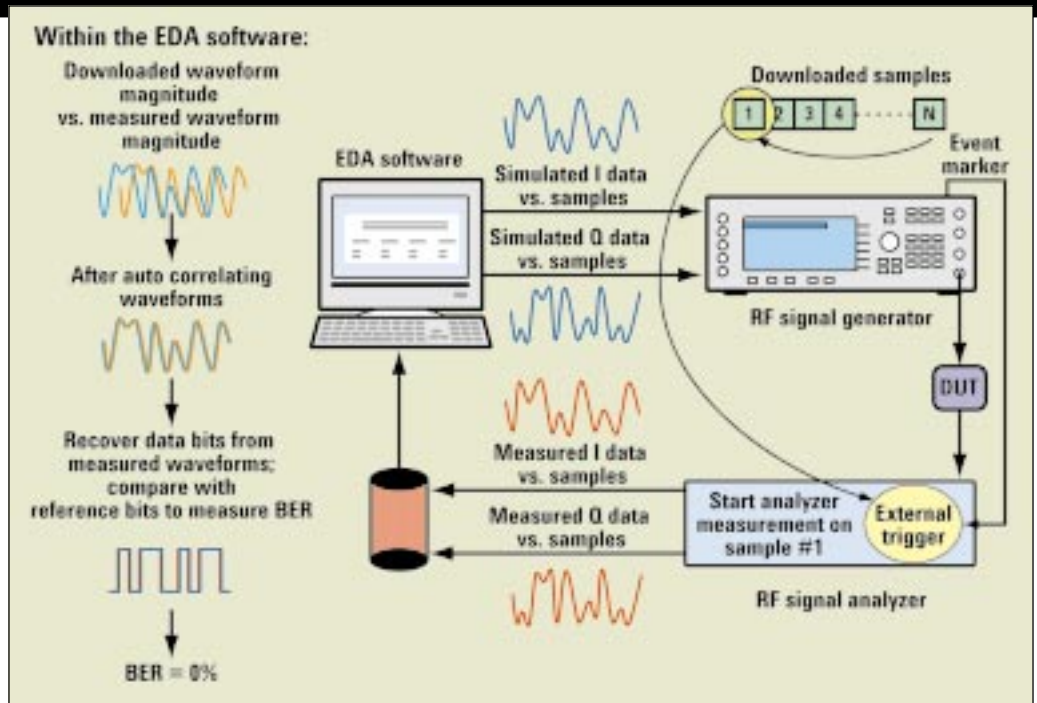


Figure 5. Time-alignment considerations in establishing a signal flow from EDA to the signal generator, through the DUT, and back into EDA from a signal analyzer.

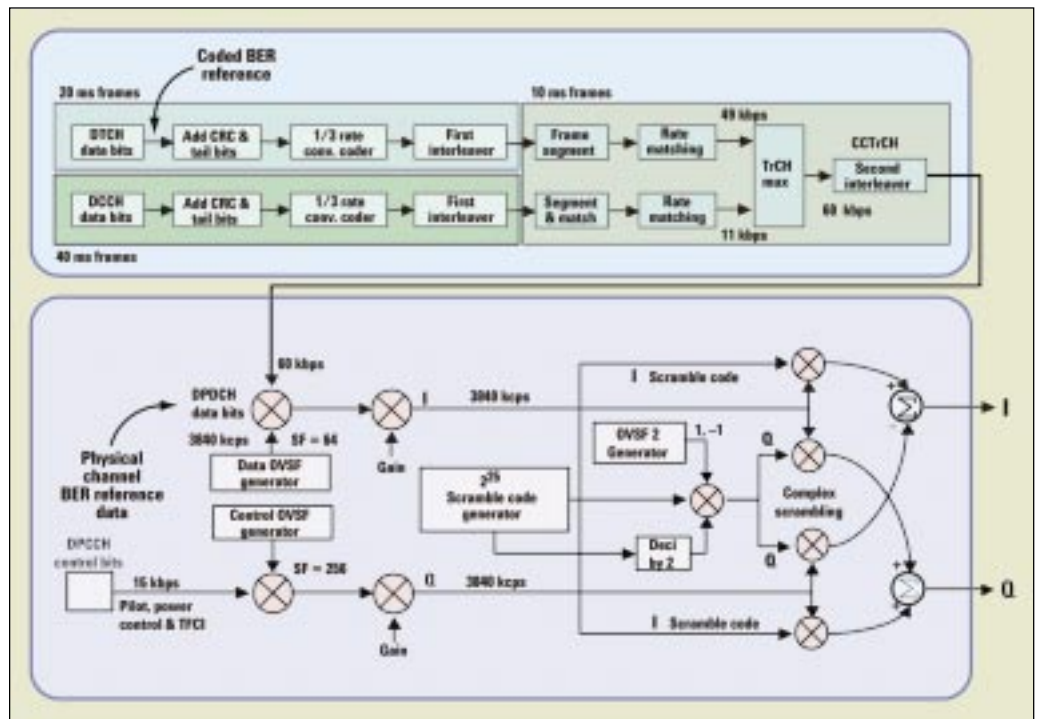


Figure 6. The coding structure for WCDMA.

As an example, let's evaluate requirements for measuring a 0.1% BER WCDMA for a 12.2 kbps reference channel configuration:

■ 0.1% BER implies that, on average, one bit error might occur every 1000 bits (0.1% = 0.001, or 1 error/1000 bits)

■ A 12.2 kbps data rate translates into 122 dedicated traffic channel (DTCH) data bits for every 10 ms radio frame (12.2 kbps\*10 ms=122 bits)

■ Counting 10 errors might require approximately 81.97 frames on average: 10 errors\*1000 bits/error\*1 frame/122 bits at a nominal 0.1% BER operating condition.

Now that a minimum number of frames required for the measurement is determined, we can evaluate the RF signal generator arbitrary waveform generator depth required to support this application.

Assuming an oversampling rate of four

samples/chip:

■ 1 frame\*15 time slots/frame \* 2560 chips/timeslot \*4 samples/chip = 153,600 samples/frame

■ 81.97 frames\*153,600 samples/frame = 12,590,592 samples to be downloaded from the EDA simulation to the signal source

Thus, for this example, 12,590,592 simulation IQ data pairs should be downloaded



Figure 7. 1000-frame WCDMA BER measurement with simulated fading using a signal source streaming data file created with an EDA simulation.

from the EDA solution to the RF signal generator to attempt counting approximately

10 errors at a 0.1% BER operating condition. In general, counting more than 10 errors may yield a more statistically meaningful BER result so downloading more than 12,590,592 IQ data pairs is desirable from a measurement accuracy perspective but requires more arbitrary waveform memory depth from the RF signal generator and a longer simulation time.

### Establishing a signal flow for analysis

The considerations discussed thus far have dealt with turning the EDA simulation signal into a real RF test signal to stimulate the DUT. The DUT output can then be analyzed in the EDA solution if there is corresponding connectivity between a signal analyzer and the EDA solution. This capability allows a complete signal flow that begins in simulation, transitions to the signal generator, passes in and out of the DUT, and now transitions from a signal analyzer back into simulation.

The same two considerations outlined for the RF signal source apply for supporting a signal flow from a signal analyzer to the EDA solution, including an additional one: time-synchronization of the EDA signal between the signal generator and signal analyzer for applications such as BER.

To support this general capability, the EDA solution must be able to accept measured data captured with a signal analyzer and create a simulation signal source from it to stimulate a design in simulation. Typically, this simulation data would be in the form of IQ data pairs as a function of time or samples, as shown in Figure 4. Also, it may be useful to support a number of different types of signal analyzers, depending on the output signal format of the DUT being tested (for example, RF/IF/analog IQ, digital, and so on).

### Measurement bandwidth

As with the signal generator, the signal analyzer must be able to support the carrier frequency and modulation bandwidth of interest. Ideally, the signal analyzer should be able to support a measurement bandwidth defined by the simulation time step used to download the EDA simulation signal to the signal generator. This helps maintain a sampling rate consistency between the EDA simulation, signal source, and signal analyzer. This sampling rate consistency helps to mitigate simulation complexities such as upsampling and downsampling when com-

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paring the signal in and out of a DUT for applications such as BER.

The signal analyzer frequency span and simulation time step are inversely related (for example,  $\text{Simulation Bandwidth} = 1/\text{Time step}$ ). It is, therefore, useful to set the signal analyzer's frequency span to the inverse of the simulation time step that was used to download the simulated signal to the signal generator arb. This can help maintain the sampling rate consistency described above.

Referring back to the WCDMA example with four samples per chip, this would imply that the signal analyzer's frequency span should be set to 15.36 MHz (4 samples/chip\*3.84 MHz) centered at the RF carrier frequency.

However, one additional consideration in setting a signal analyzer's frequency span to establish a desired equivalent time step may be a cardinal span factor,  $k$ , where the  $\text{TimeSampleResolution} = k * \text{FrequencySpan}$ .<sup>1</sup> For example, if the cardinal span factor were 1.28, then the signal analyzer's frequency span would instead be set to 12 MHz (15.36 MHz/1.28) instead of 15.36 MHz. If the EDA solution link to the signal analyzer is capable of resampling the measured data to establish a user-specified simulation time step, then this may not be as critical.

These types of considerations will vary depending on whether an RF signal analyzer, logic analyzer, or oscilloscope is used to capture the DUT output. For a DUT with a digital output (such as a receiver with analog-to-digital converters at its output), the signal would be digital and the RF carrier frequency and frequency span consider-

ations would not necessarily apply<sup>2</sup>.

The maximum number of measured IQ data pairs that can be read from the signal analyzer to the EDA solution can also be an important consideration, particularly for receiver BER or PER applications.

Note that for applications such as BER or PER, the signal generator should be capable of effectively capturing all of the data that were downloaded from the EDA software to the signal generator to test the DUT. Typically, the measured data being read from a signal analyzer into the EDA simulation solution would be sampled I and Q envelope data, which would be remodulated onto an RF carrier frequency within the EDA solution.

### **Time-synchronization of the EDA signal**

A key consideration in supporting an overall signal flow from simulation to test and back into simulation is the time synchronization of the EDA signal between the RF signal generator and RF signal analyzer.

An application example is BER or PER, where the bits into the DUT must be compared to the bits out of the DUT to compute BER. This involves comparing bits in and out of the DUT sequentially, which implies a time alignment of the bits being compared. From an EDA solution/test equipment interface perspective, it implies time-alignment of the IQ waveforms created/analyzed in simulation as the simulation-defined signal transitions to the signal generator and from the signal analyzer.

For example, Figure 5 shows an illustration of the time-alignment considerations. Note that this is a conceptual representation, so the I and Q waveforms out of the signal analyzer don't reflect any magnitude or phase differences relative to the I and Q waveforms downloaded to the signal generator.

There are two levels of time synchronization to be considered: (1) synchronizing the playback of the simulation IQ waveform in the signal generator with the signal analyzer's measurement and (2) removing any residual physical delays from the DUT prior to performing a measurement, such as BER, with the EDA software.

To accomplish the first level of time synchronization, it is important to have an event marker output on the signal generator that outputs a pulse when the first sample of the simulation IQ data is being output (beginning of the Arb sweep). This allows the signal analyzer's measurement to be externally triggered on the occurrence of the signal generator's event marker such that the measurement/data capture starts at the beginning of the Arb sweep<sup>3</sup>. This is shown in Figure 5 as a physical connection between the signal generator's event marker and signal analyzer's external trigger.

To accomplish the second level of time synchronization, the simulated IQ waveforms downloaded to the signal generator need to be time-aligned with the measured IQ waveforms captured with the signal analyzer. Even with the first level of time synchronization discussed above, additional time delays can result from the physical delay of the DUT and cables. This is illustrated in Figure 5 on the left side, where the blue trace represents the magnitude of the simulated waveform created in the EDA solution and downloaded to the signal analyzer Arb, referred to as the *reference waveform*. The red trace represents the magnitude of the DUT measured waveform read back into simulation from the signal analyzer, referred to as the *test waveform*. The time misalignment between them reflects the physical delay of the DUT and cables. Time alignment of the reference and test waveforms must then be performed in the EDA simulation, either manually or automatically, prior to recovering the data bits from the test waveform and comparing them to the reference data bits for BER

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computation. A manual time alignment can be tedious and time-consuming, so it is generally desirable to perform this with a simulation auto-correlation algorithm or something equivalent in the EDA solution.

For applications such as BER or PER, the signal downloaded from the EDA solution to the signal generator should reflect the coding structure of the signal format of interest. For example, the coding structure in Figure 6 reflects the coding that should be applied in the EDA solution prior to downloading the simulation signal to the signal generator Arb. For example, the reference bits in a WCDMA-coded BER measurement would be the data traffic channel (DTCH) data bits on the upper left, before applying CRC and tail bits, convolutional encoding, interleaving, spreading, scrambling, and so on, in the EDA solution.

On the receiver side, the EDA solution would need to post-process the measured signal from the DUT output (read from the signal analyzer) to effectively remove the

based signal generator solution, so a streaming data file was created with EDA simulation and the simulation data was then streamed from the data file to the RF signal generator.

Note that the uncoded (physical) BER measurement is degraded by the simulated fading environment at this RF power level and does not achieve stability until after about 450 frames of data—450 frames of data is more than can be accommodated by an arbitrary waveform generator memory depth of 64 Msamples at an oversampling rate of 4 samples/chip. The coded BER and block error rate (BLER) are 0% at this RF power level.

### **Summary**

Numerous technical details must be considered when using combined EDA simulation and test equipment to tackle application problems. While they may seem challenging at first glance, the basic considerations discussed in this article can be applied from

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## *The basic technology to combine EDA solutions with test equipment solutions has evolved significantly over the last few years and has enabled new applications to be addressed, such as BER/PER.*

coding applied in the signal creation. Specifically, after the signal analyzer signal has been read into simulation, the EDA solution would need to post-process it to descramble, despread, de-interleave, decode and remove the CRC and tail bits to recover the DTCH data bits from the measured signal. Once the DTCH data bits have been recovered, they can then be compared to the reference data bits to perform the BER measurement.

One of the benefits of combining EDA solutions with test equipment solutions for signal creation and analysis is the flexibility offered by simulation. Impairments can be modeled in simulation and the impaired simulated IQ signal can be downloaded to the RF signal generator Arb to test a DUT. Likewise, custom signal formats can be created and analyzed in simulation using the capability discussed here, if working with emerging or proprietary signal formats.

An example is shown in Figure 7, where a fading profile impairment is applied to a WCDMA signal in simulation before turning it into an RF test signal with an RF signal generator configured for data streaming. In this example, the amount of data required exceeded what was possible with an Arb-

one application measurement to the next. These concepts can also be applied with different types of test equipment, depending on the application problem to be solved. For example, the time-synchronization issue for the RF signal generator and RF signal analyzer can also be applied to an RF signal generator paired with a logic analyzer for mixed-signal receiver measurements where the output is digital instead of RF.

The basic technology to combine EDA solutions with test equipment solutions has evolved significantly over the last few years and has enabled new applications to be addressed, such as BER/PER. If this is any indication of future trends, then perhaps combining EDA and test solutions together may be key to addressing tomorrow's emerging design and verification challenges quickly and with flexibility. RFD

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