

Si integration with millimeter wave phased array antenna

Radiating aperture and beam-forming networks are key components of advanced military and commercial wireless systems, and new technologies are needed to meet the desired performance goals.

By Fred Mohamadi

To achieve a reliable, efficient and high-speed Wireless LAN (WLAN, IEEE802.11) and wireless metropolitan area network (WMAN, IEEE802.16) a system must provide the following characteristics:

- Electronically beam steerable for quick switching between terminals and to minimize multipath effects.
- Wide bandwidth to accommodate high throughput rates.
- Sufficient power capabilities to ensure adequate received power levels maintaining constant robust communications link. However, radiated power intensity must not exceed safety limits.
- Narrow beamwidth to permit angular diversity usage.
- Small, lightweight, low profile and conformable to desired surfaces for suitable use in portable systems.
- Provides simple and flexible setup with minimum usage of wire connections to fixed structures such as walls and ceilings.
- Withstand interference from human movement and noise from other network sources.
- Suitable for use with higher millimeter-wave frequencies.

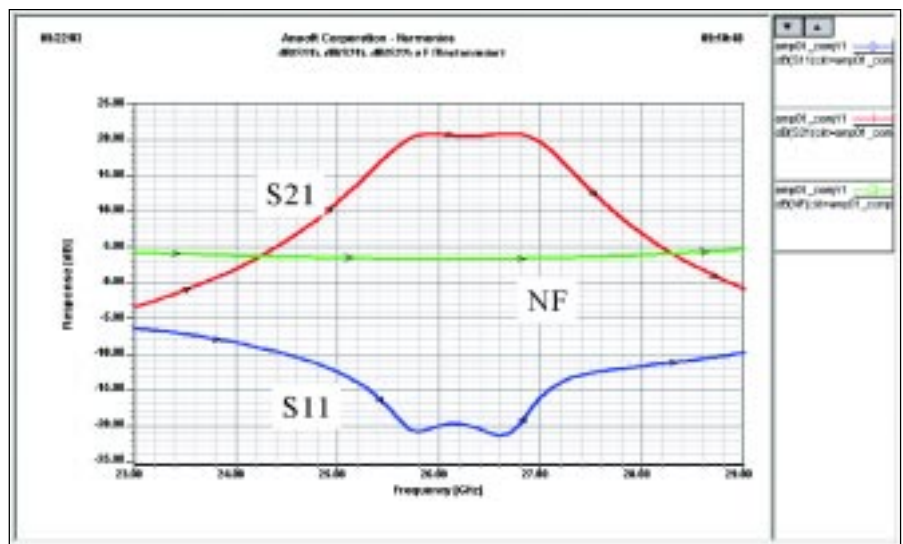


Figure 1. Ka-band amplifier portion of the IAPMC chip.

- Low cost is an essential requirement.
- An integrated antenna and RF receiver system with an electronically programmable phase management chip can be used efficiently in wireless LAN/MAN, RF asset management systems (tag and interrogator),

radiometry and passive imaging, and satellite communications operating at millimeter-wave frequencies.

Beam-forming technology

With higher frequencies and the potential

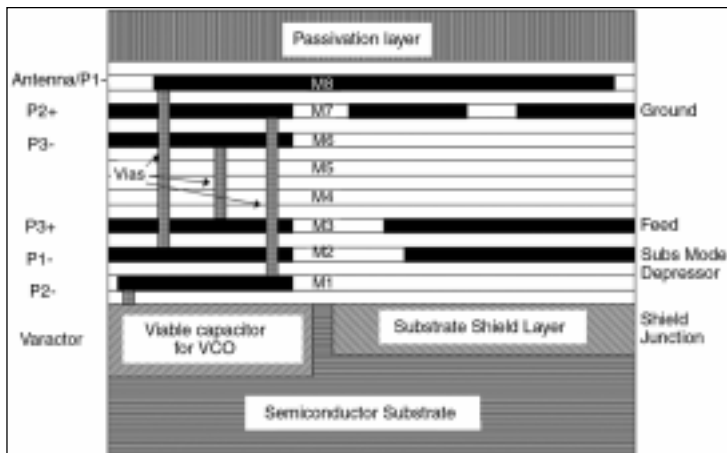


Figure 2. Integrated antenna implementation for receiver.

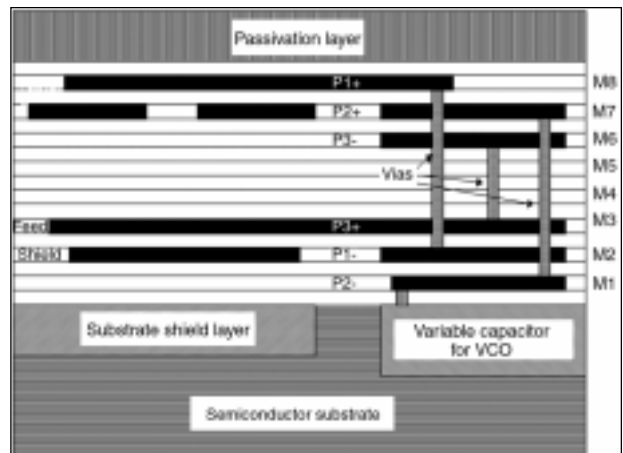


Figure 3. Integrated antenna implementation for transmitter.

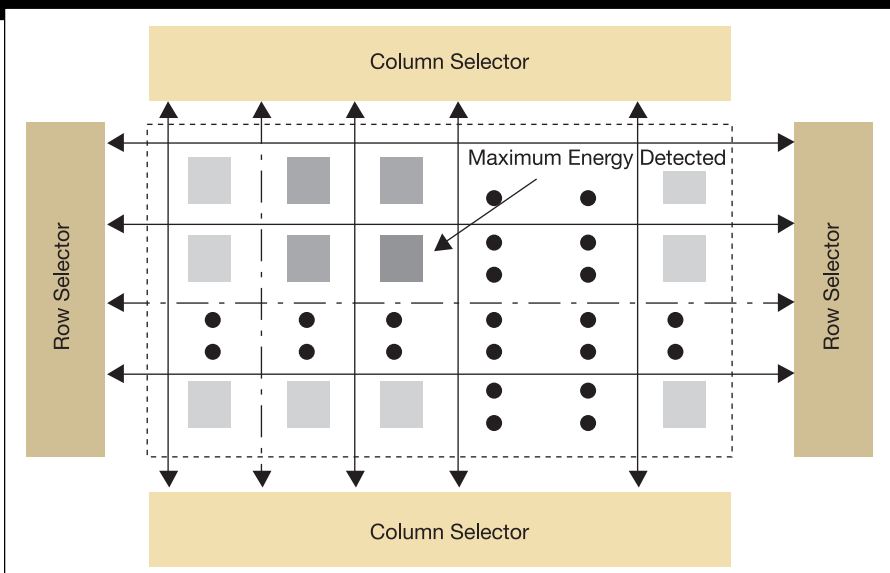


Figure 4. Programmable phase management array for spatial diversity.

development of a hybrid analog DSP configuration has significant advantages in power and cost reduction. Using an antenna array system with a hybrid analog-digital beam-forming network enables separating the tasks to throughput intensive (addressed in RF) and computation intensive (using DSP).

Integrated antenna and phase management chip

Application of integrated antenna and phase management chip (IAPMC) is being evaluated in a number of related fields such as power combining, beam steering and switching, retrodirective arrays—to be combined with high-efficiency power amplifier designs [2,3]. These IAPMC-based designs are expected to be particularly attractive for millimeter-wave systems because they provide an effective solution to several fundamental problems at these frequencies, including high transmission-line loss, limited source power and reduced antenna efficiency. IAPMC must also provide a less complex and high-performance phase shifter in lieu of the common corporate feed network.

Stand-alone antenna oscillators have inherently low stability. The combination of a single, active device oscillator with an antenna that generally has a bandwidth of a few percent results in an external quality factor less than a few 10s. While this may be

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of using higher data rates and higher user density, multipath fading and cross-interference has become a serious issue, resulting in degradation of bit error rate (BER). To address these problems and to achieve higher communications capacity, antenna array systems with adaptive beam-forming capability have proven to be effective in suppression of the interference as a result of multipath signals [1]. Digital beam-forming systems consist of a digital signal processor (DSP) that calculates and applies weight vectors to each sampled data. The approach has the disadvantages of complexity, however, it provides more flexibility at the cost of high power dissipation. Additionally, current DSP technology has a speed bottleneck in data I/O. Operating at X, K and W band requires massive use of analog-to-digital and digital-to-analog converters (ADC and DAC) and DSPs. The real-time applications require parallel efforts from the relatively slow individual DSPs (relative to frequency of the received signal).

To overcome this problem,

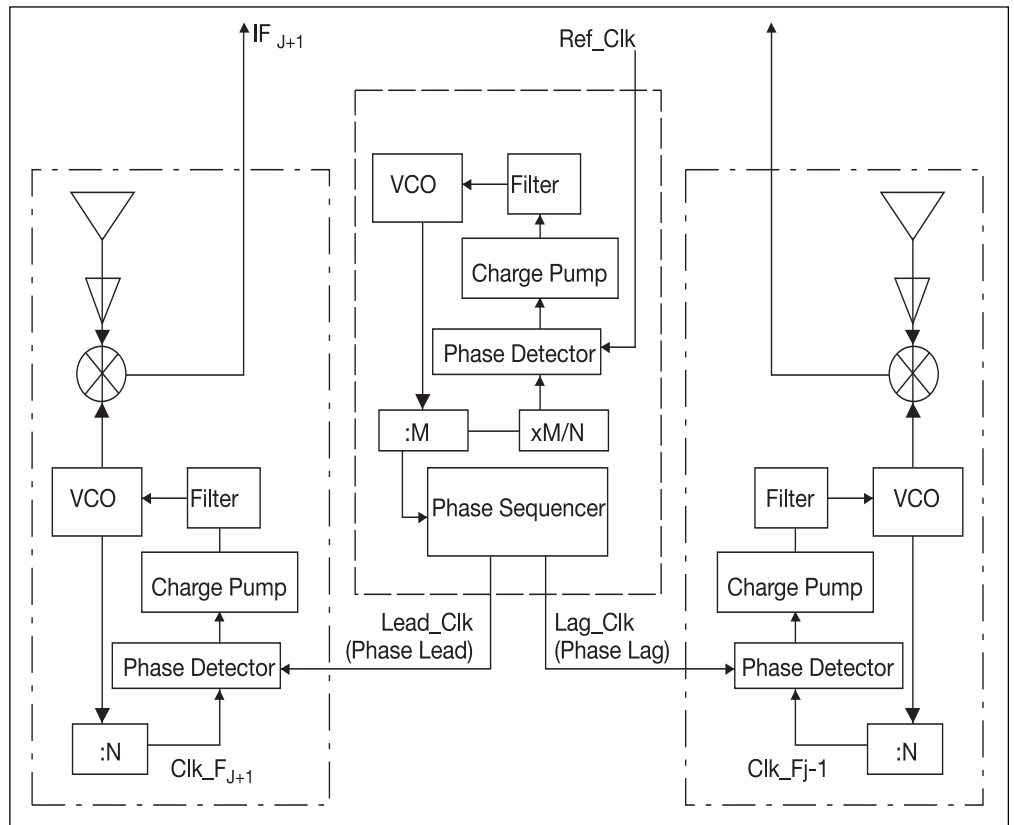


Figure 5. Proposed programmable phase management system.

acceptable in short-range sensor systems, such as alarms or collision avoidance systems, it is too low for most multichannel communications applications. In addition, long-term stability must be improved and tuning made more accurate. A coupled cavity beneath the antenna oscillator has been demonstrated [4]. One specific design [5] consists of two stacked silicon substrates: a) the top substrate, which carries the microstrip antenna, is micromachined to improve the radiation performance of the antenna and b) the bottom substrate, which carries the microstrip feed line and the coupling slot. The measured return loss was -18 dB at 94 GHz, and a 10% bandwidth at -10 dB cut-off point was reported. Implementation of an antenna by using exotic methods (including micro machining) is not cost-effective. Significant progress in design of high-speed CMOS- and SiGe-based (10 to 40 GHz) phased-lock loop (PLL) techniques has been reported recently [6-8] that enables use of a reference clocking system to lock the voltage-controlled oscillator (VCO) for better stability.

Figure 1 represents simulation results for design of an amplifier at the receiver of an IAPMC. The collected radiation on the top plate of the antenna is coupled to input stage for automatic gain control circuit, down-conversion and amplification [7]. The IF signal is then delivered to a data converter and DSP unit. A multiport monolithic transformer, shown in Figure 2, acts as the coupler and isolating bandpass filter to a receiver. In a separate micro winding pair that couples to the antenna (Figure 3), the micro transformer acts as the isolating circuit for the transmitting signal in another frequency band.

Shown in Figure 3 is the multilayer metalization for implementation of a stacked antenna patch. A standard semiconductor process (future generations of SiGe process 9HP from IBM) can be used to address full integration of IAPMC and RF circuits. Aluminum or copper is patterned in spiral shapes at submicrometer separations from each plane.

Figure 3 shows a patch antenna implemented using an 8-metal layer Si-based process. Metal layers M1 through M8 are formed using a 100 to 120 micrometer substrate that includes a doped substrate shield layer. Silicon dioxide layers separate the metal layer M1 through M8 in a standard manufacturing process. Feedline is formed in lower metal layer M2, a shield to substrate is patterned in metal layer M7, and a patch element is defined for upper metal layer M8. A low-dielectric passivation of thickness of few micrometers is formed on upper metal layer M8 to prevent environmental corrosion.

Although the shown implementation is for an 8-metal layer Si-based process, it can be appreciated that the patch antenna requires

only a 3-metal layer semiconductor process.

As seen in Figure 3, the dimensions of patch, aperture and feedline depend on the desired operating frequency. For example, feedline may have a width of 30 microns, while the patch element may be 500 to 1000 micron (or micrometer) length depending on the carrier frequency of 50 to 100 GHz.

Figure 4 shows the proposed architecture to address signal exchanges between antenna array elements. A low-speed bus feeds digital information that a sequencer will use to generate proper phase. The concept is similar to the row and column selections that are designed in standard semiconductor memory products such as static random access memory (SRAM). A key element in the design of the array is proper isolation of the antenna elements from intercoupling. Unique isolation technologies such as ground plating deep trench pattern or laser cutting can be incorporated for prevention of inter-antenna coupling as well as the substrate coupling.

Phase management system design

Figure 5 shows a block diagram of a master PLL. A reference clock (Ref_Clk) is supplied from a stable source such as a precision crystal oscillator. The locking of the VCO to this reference clock will provide enhanced phase noise. The output of the natural oscillation frequency will be divided by N times such that it can be compared, phase-wise, with the reference clock. A signal is also generated for the sequencer by a divider M . In a typical application, the sequencer can be a binary-based counter with N/M resolution, which delivers incremental phase expansion/contraction between the Ref_Clk and Lead_Clk and Lag_Clk, respectively. For a 40 GHz PLL and a 625 MHz Ref_Clk, N is 64. For an 8-bit phase resolution, $M=8$ corresponds to a 5.0 GHz sequencer clock. A practical $M=16$ can be designed using both clock edges at 2.5 GHz. This clocking scheme can be implemented using a 0.09 micron (or 90 nm) CMOS process. Power consumption of such a PLL/synthesizer is estimated to be below 100 mW. Phase detectors then produce signals indicating a lagging or leading relationship with respect to the Ref_clk. The continuous phase change by sequencer provides proper accurate signals with known phase for beam steering or frequency shifting applications. The lead and lag clocks are then used to act as the reference clock that feeds the PLL of the slave antenna arrays. Relative increment of phase shift for each PLL is achieved with respect to the master Ref_Clk.

VCOs are used in conjunction with mixers to perform downconversion during scanning or receiving the RF signals at various channels (or sub-bands). For example, an

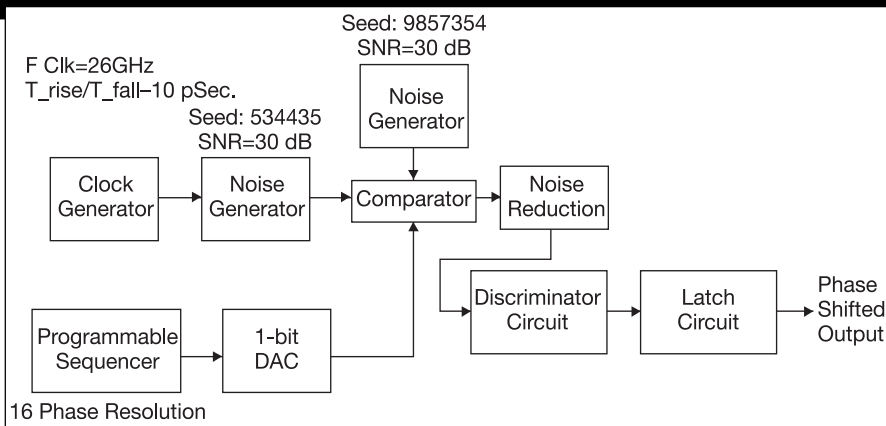


Figure 6. Programmable phase management/sequencer chip.

integrated scanner with 4 X OC-12 sub-band channels (25 to 27.5 GHz) using integrated antenna and downconverters with controller, power manager unit and a synthesizer is estimated to consume less than 650 mW for a 1.8 V supply (0.18 micron standard SiGe process). This power consumption can be further reduced using system sleep mode and on-demand function based on detection of radiating signal. As a result of a small duty cycle, the durability of battery-operated systems can increase by a few orders of magnitude. For beam-steering scanners, if the repetition period of the master VCO is 38 ps (26.0 GHz), the expected phase step for a desired 8-bit phase resolution is then $(38 \text{ ps} - T_r - T_f) / 8 = 2.8 \text{ ps}$. Implementing a 26.0 GHz VCO (in a 0.18 micron SiGe technology) with 22 mW core power indicates a PLL measured RMS jitter of better than 0.25 ps corresponding to a total jitter of 3 ps (Figure 7). Accordingly, effective beam steering is expected to have an electrical phase resolution of $180:8=22^\circ$, while a 3 x 5 element antenna array has 15° beamwidth.

Phase management function

Figure 6 represents the architecture of a phase shifter system used for simulation of Lead_Clk delivery. A ramp generator, a dynamically programmable sequencer and a comparator are used to manage the phase adjustment portion. Additionally, three sources of noise are used to simulate the jitter and amplitude degradation at the presence of server noise.

A digital-to-analog converter provides an analog level to be compared with the time elapsed from the reference ramp generator. Output of the comparator is then fed to an integrate-and-dump circuit and is being compared to a level detector. Upon meeting the set voltage detection limit, the signal is then converted to a binary stream and fed to a neighboring integrated antenna unit as a reference clock.

Figure 7 (a) demonstrates the simulated output of the described circuit running at 26 GHz for CMOS or SiGe implementation.

The simulation was done while the noise reduction circuit was disabled. Addition of the noise-reduction circuit enables significant improvement in clock shaping as presented in Figure 7 (b). The improvement depends on the power budget and available transistor's f_{max} for design of the phase shifter such that the rise and fall times can be as small as possible at these speeds.

Figure 8 contains snap shots of angular beam position, its beamwidth (at -3 dB from peak), and its radiated field for 1 V signals launched to a 50 ohms terminations of an array of antennas.

The selected frequency for this simulation was 26 GHz, and the designed dimension of the 4-element array measured only 16 mm x 16 mm (W x L). The simulation results show a gain of 14.7 dBi at resonant frequency of 26 GHz. No optimization by matching impedance to enhance the antenna element S11 was performed. This will simulate worst-case condition of detuning. Its radiation pattern provided a -3 dB beam bandwidth of 40° with major grating lobes at -24.2 dB level at offsets of 60° for zero "phase shifting" case. Furthermore, the gain of 4 x 4 elements within the 16-element (orthogonal pairs) array was 21 dBi, up from 15 dBi of a 2 x 2 array, which demonstrates nearly 6 dB power combining efficiency of the quasi-optical power technique.

Conclusion

Demand for wider-than-GHz bandwidth for wireless systems is growing to address the bottlenecks of Gbps and beyond data rate pipelines. Antenna dimensions are shrinking as applications of wireless systems move to millimeter-wave ranges. The size convergence of the submillimeter-wave length antenna size and dimensions of active devices above tens of GHz of operation evolves to integration capability of the antenna and RF circuits in the same substrate. Current semiconductor-based implementation of the RF devices with the antenna can provide orders of magnitude reduction in cost, size and enhancement in performance due to the reduction of losses associated with the discrete implementations. The availability of a radio the size of a sugar

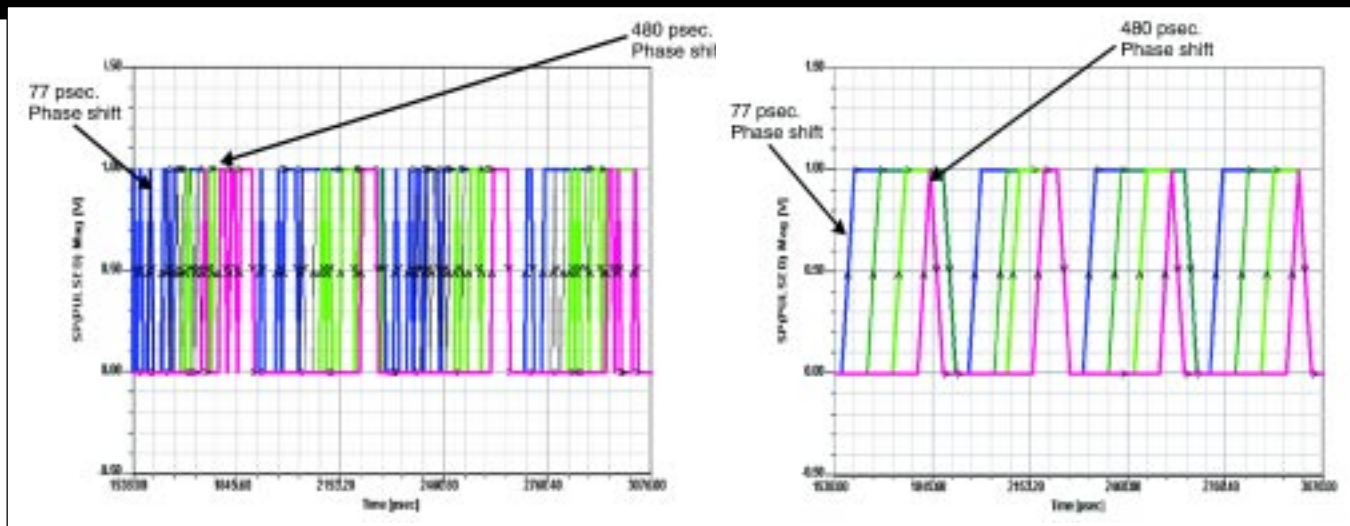


Figure 7. Phase shift output simulation at Ka-band—(a) server noise environment (b) with noise reduction function.

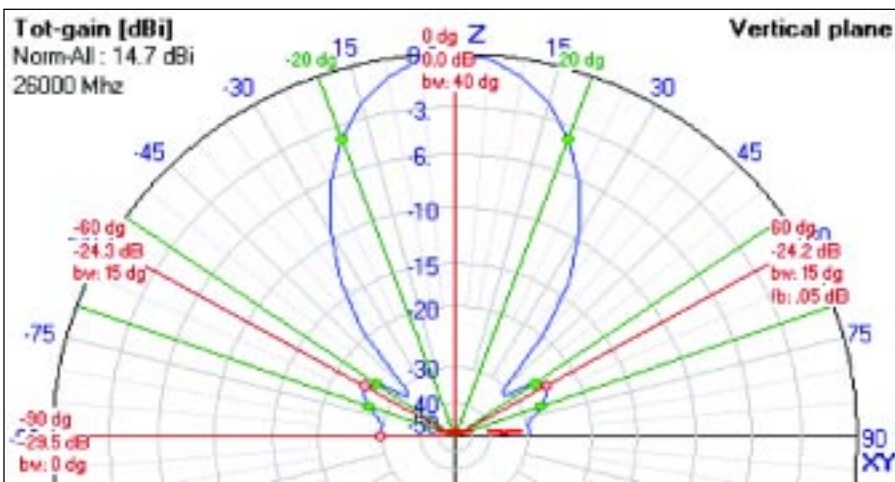
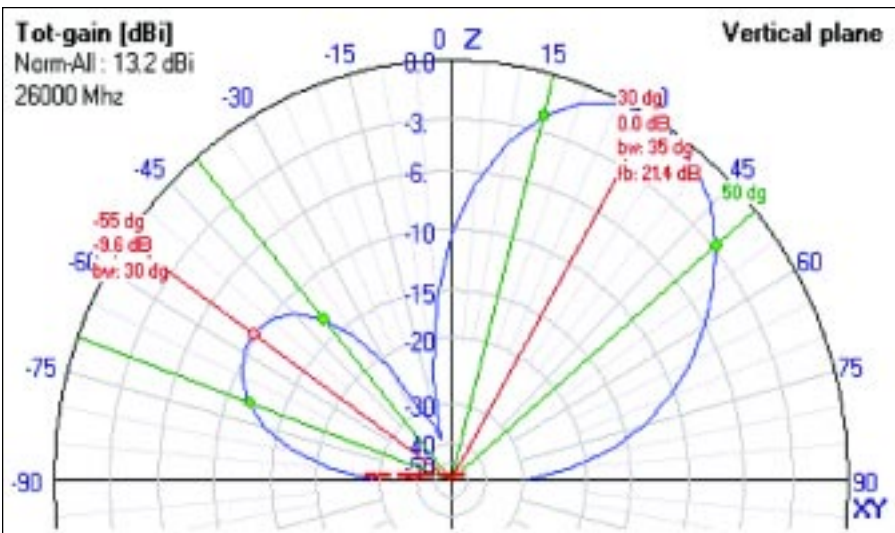


Figure 8. Beam steering function of IAPMC—(a) 2 x 2 array, Theta 0°, 14.7 dBi antenna gain, beam width 40°.



(b) 2 x 2 array, Theta 30°, 13.2 dBi antenna gain, beamwidth 35°.

grain will be a reality in the next three years. RFD

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