Space-grade DC-DC converter revolutionizes low-power RF design

A space-grade multiple output DC-DC converter design platform offers high performance and cost benefits with established assembly outlines for most custom requirements.

By Tiva Bussarakons

Standards for power requirements and form factors for equipment designs do not exist for space applications. Major satellite manufactures establish their own power bus standards, the main power line that regulates the power from the solar panels and delivers regulated voltage to all the payload and system equipment. Most have a unique input/output voltage range, voltage level and dynamic behavior, telecommand (TC) and telemetry (TLM) interfaces among the subsystems that are also distinctive. The converters' output voltages and powers while dictated by the types of load are often unique from one payload design or program to the next. The distinction or lack of standards is believed to be due to the competitive nature of the industry. Each manufacturer attempts to gain a competitive edge on functional performances and overall power conversion efficiency resulting in unique designs and the lack of similarity in power converters.

IR's Mx design platform is created with these diverse input, output, and functional requirements in mind. In addition to insistence for high efficiency and functional performances, the space industry when making any make/buy decisions for a DC-DC converter for new equipment designs, demands design documentation/analyses and flight heritage to mitigate program risks that may cause slippage in delivery schedule and added costs.

This design platform targets low RF power design applications requiring power up to 15 W. The platform is developed for sensitive RF equipment onboard a spacecraft, i.e., receivers, transmitters, beacons, low-noise amplifiers (LNAs), and up/downconverters. It is designed for continuous operations in radiation environments that are presented to commercial, military and scientific missions operating in long-term geosynchronous (GEO), medium earth (MEO) and low earth (LEO) orbits.

Platform description

Mx series is a radiation-hardened multiple outputs DC-DC converter design platform that can be adapted to most satellite input and output power requirements. The design topology allows simple component changes in the primary section to accommodate different bus voltages. While most design applications require power up to 15 W, the platform has adequate design margin to accommodate slightly higher combined output power than 15 W. The platform includes TC/TLM design that can be readily adapted to most major satellite interface requirements. It also includes a hold-up capacitor bank and electrical circuitry to insure proper turn-on and turn-off timing among the outputs, a critical biasing sequence for GaAs FET devices commonly used for RF power amplifiers.

Two standard assembly outlines exist. While MA platform is for output power up to 5 W, MB with a slightly larger outline is for output power of up to 15W. Open board PCB-style construction is chosen to facilitate design adaptation and design changes as needed. Proprietary design simulation tools and design analysis templates are created to quickly and accurately provide performance projection and design trade offs where decision in design changes can be made with a high level of confidence. The platform offers RF equipment designers the ability to react and incorporate last-minute design adjustments with little or no impact to program schedule.

Platform design benefits

In addition to deliverable hardware, i.e., engineering model (EM), engineering qualification model (EQM), protoeflight model (PFM), and flight model (FM), almost all space programs require extensive design, qualification and program documentations. These items typically include preliminary/critical design review meetings, thermal analysis, stress analysis, reliability analysis, worst case analysis, failure mode effect analysis, radiation susceptibility analysis, acceptance and qualification test procedures/reports, monthly program reports, updated program schedule, weekly status update, and dedicated program management function.

These deliverable items, program review and design review meetings can incur substantial costs and impact program schedule and may become the pacing items when design changes occur. The Mx design configuration and the proprietary simulation and design tools are primed to lessen these impacts.

Key performances and features

Performances and functional features of

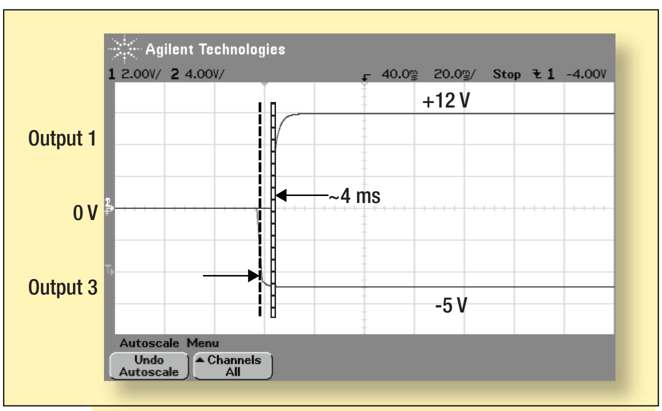

Figure 1. Outputs timing during turn-on, output 1 (+12 V) vs. output 3 (-5 V).

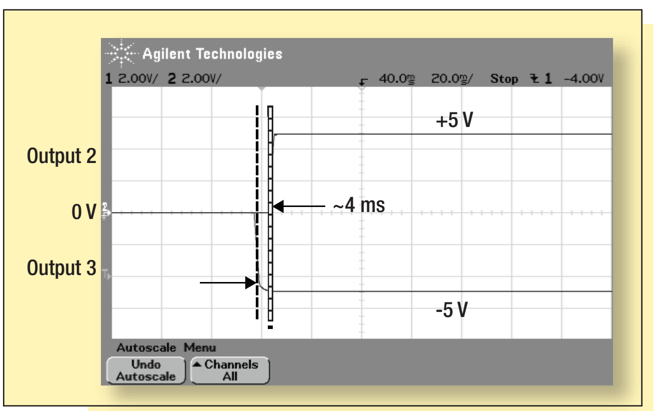

Figure 2. Outputs timing during turn-on, output 2 (+5 V) vs. output 3 (-5 V).

Mx series can be summarized as follows:
- accommodates most major power buses, 28 V, 50 V, 70 V, and 100 V;
- integrated input filter to ensure EMC/EMI compatibility to most satellite power buses;
- no limitation on number of outputs though most requirements are triple output configuration;
- each output can be configured to meet output voltage levels up to 15 V and any current level up to 1 A;
- guaranteed voltage accuracy and regulation to within 1% begin-of-life and 2% end-of-life accounting for temperature, radiation and aging effects;
- no cross regulation and crosstalk as each output is independently regulated;
- two design patents are deployed to maximize efficiency performance;
- efficiency is in the range of 65 to 75% depending on output voltage, current and power;
- each output uses linear regulator enabling output noise to be less than 1 mV(RMS);
- conducted susceptibility (CS) rejection is as high as 100 dB as a result of a two-stage regulation design;
- outputs are orderly sequenced during power-up and power-down to insure proper biasing for RF amplifier devices;
- isolated on/off tele-command and on/off status telemetry with a latching relay;
- two established assembly outlines for differing output powers; and
- components are space flight qualified class S.

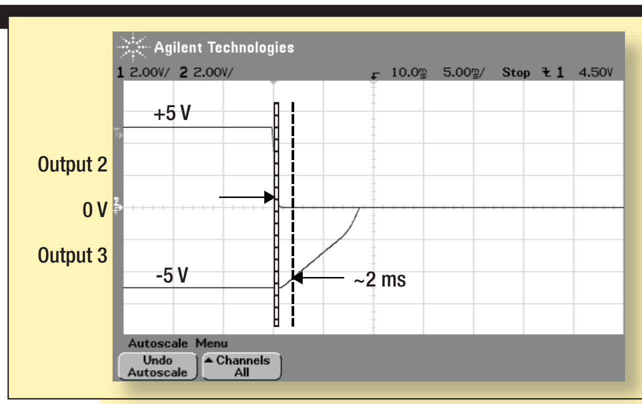

Figure 3. Outputs timing during turn-off, output 1 (+12 V) vs. output 3 (-5 V).

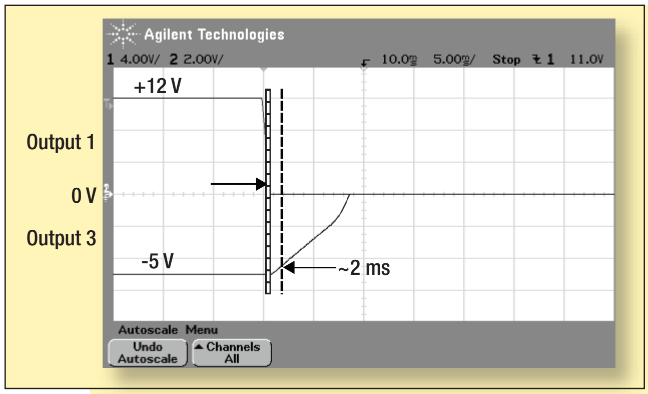

Figure 4. Outputs timing during turn-off, output 2 (+5 V) vs. output 3 (-5 V).

Actual performance

Waveforms, **Figures 1-4**, taken from products delivered to customers are samples of the actual performances.

Design description

Functional block diagram shown in **Figure 5** represents the design topology for the MA and MB platforms. The shaded blocks highlight the differences. They include the primary power stage, power transformer and output rectification scheme. While triple output designs are common for most applications, the platform can be configured to accommodate any number of outputs with the limitation being the total combined output power requirements.

Design Topology

The MA and MB designs deploy dual voltage regulation stages, one in the primary and one in the secondary. Regulation in the primary uses current-mode control topology to maximize efficiency. The topology offers inherent current regulation and primary overcurrent protection. Regulation in the primary is built around a standard PWM controller with known performance characteristics in the targeted radiation environments. Voltage regulation is performed on the internal 10 V supply via a bootstrap winding of the power transformer (XFMR). All primary circuitries including the PWM controller and gate drive circuitry are powered by an internal 10 V linear regulator upon power up. The internal 10 V supply takes over all biasing responsibility upon achieving regulation. All primary input circuitries are galvanically isolated from the secondary output via a power transformer. Secondary voltages of the transformer are stepped down, rectified and filtered feeding downstream output regulators. All outputs are independently regulated by linear voltage regulators, which offer inherent excellent noise and regulation performances. The regulators use discrete components with a bipolar transistor as a pass element to minimize voltage headroom and maximize efficiency. The regulator circuit is a proprietary design that has been used successfully for many design applications. Extremely low output noise and high CS rejection are possible with the dual-stage regulation scheme. Guaranteed end of life performances for voltage accuracy and regulation can be demonstrated through worst- case and aging design analysis.

Input/output power train

The single-switch flyback and two-switch half bridge can accommodate a wide range of input voltages. The switch elements are selected based on the operating input bus voltage and dynamic transient conditions. Transformer design and turn-ratios are adjusted accordingly. The output rectifiers may require different voltage and current ratings. MA and MB assembly outline designs have taken into account all the changes in component footprints due to the deviations in input and output requirements. The established PCB layouts and dimensions can normally be maintained for most design applications.

The Mx platform also includes an input filter design that yields very low reflected line noise and is expected to satisfy EMI/EMC requirements of most major satellite power buses. While the design will change to accommodate different input bus voltages, the change in the filter components have little or no impact on the assembly layouts.

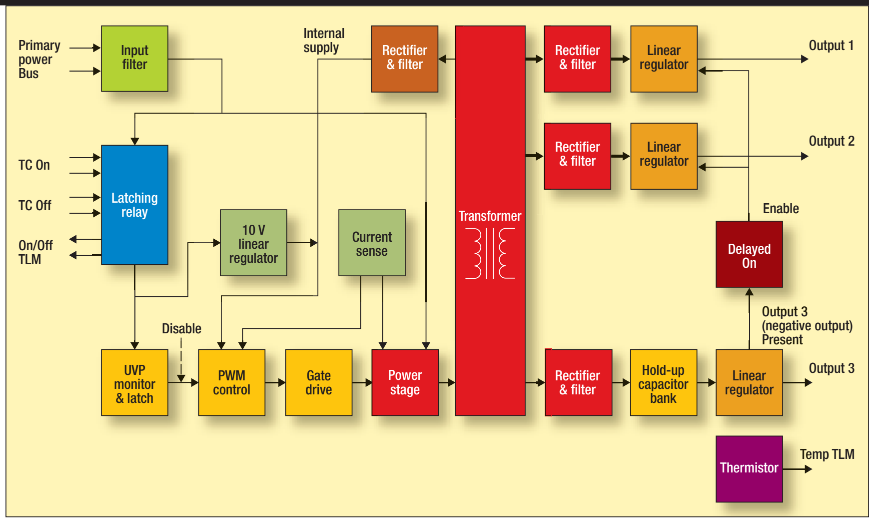

Figure 5. Mx series functional block diagram.

The TC/TLM interface will accommodate a standard high-level pulse command using latching relay to provide the necessary isolation. The telemetry on/off status is bi-level. The TC/TLM interfaces are isolated from one another and from any other functional and input/output terminals within the converter. Temperature telemetry is available and can be included as required.

References

1. U.S. Patent No. 4 899 271.
2. U.S. Patent No. 5 335 163.

ABOUT THE AUTHOR

Tiva Bussarakons is marketing director for International Rectifier. He joined the company in 1999 as field application engineer. He has been marketing director for the dc-dc converter product line of the HiRel Product Group since 2002. Bussarakons holds a BSEE and an MSEE from California State Polytechnic University at Pomona, and an MBA from Pepperdine University at Malibu, Calif.