

# Fully integrated CMOS transmitter design considerations

Traditionally, multiple IC chips are needed to build transmitters (Tx) used in wireless communications. The difficulty with a full Tx integration is that each Tx building block uses different technology. A power-detection circuit will exploit the Schottky diode, while the modulator IC is integrated with BiCMOS or SiGe. Likewise, the digital control loop is implemented in CMOS. Now that direct-conversion Tx uses digital control loop for nonlinearity corrections, CMOS technology can provide the route to a fully integrated Tx.

By Louis Fan Fei

**A**lthough, CMOS technology itself can't compete with GaAs, HBT, SiGe or BiCMOS technologies, a CMOS Tx can be integrated with a powerful DSP. Thus, by using DSP many CMOS deficiencies can be alleviated. For example, by using a predistortion technique for a PA along with the DSP, the nonlinearity problem can be dramatically improved. For an efficiency-related problem, the techniques such as polar loop, Doherty, dynamic bias or linear amplification with nonlinear components (LINC) can improve the performance. The major building blocks in a highly integrated Tx are a PA, a modulator (MOD), a power detector (PD), an automatic gain control circuit (AGC) and the voltage-controlled oscillator (VCO). Typical implementation of each of these blocks will be discussed.

## Power amplifier

The CMOS PA has gradually replaced the HBT or GaAs FET in the low to medium (up to 20 dBm) power applications like Bluetooth and WLAN at 2.4 GHz to 2.5 GHz and 5.1 GHz to 5.9 GHz. For a CMOS IC, the common-mode noise is an issue. The differential configuration is the answer. The output power can be combined at the final stage with a balun or left it as a differential interface if the post PA SAW is balanced or a dipole type antenna is used.

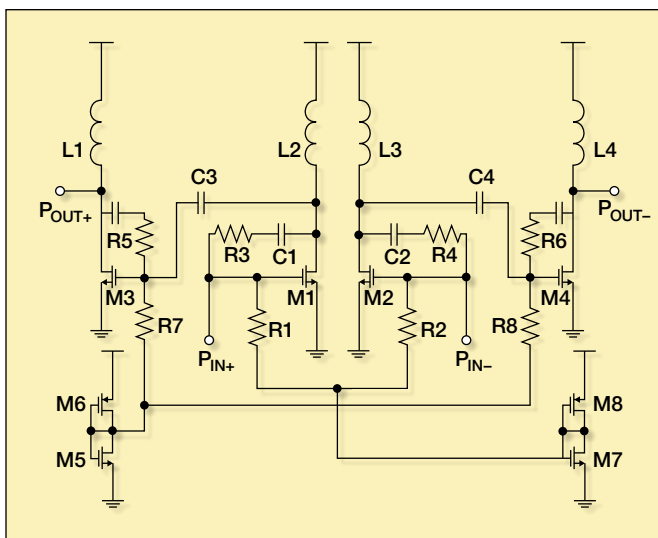


Figure 1(a). Differential CMOS PA.

A PA design's emphasis is on the output power, power gain, linearity and efficiency. The design starts at the output port where the output power contours of the device are characterized. Once the output termination is determined, the matching circuit is designed the same way as the other RF building block's matching circuits. A two-stage common-source FET with the RC feedback is shown in Figure 1(a). M1 and M2 are the driver stages. M3 and M4 are the output power stages. RC feedback from the drain to the gate stabilizes the transistors at the high frequency. The feedback also widens the bandwidth of the PA. M5 and M6 and M7 and M8 are the active resistive dividers to bias the driver stage and the power stage, respectively. The cascode PA design is popular as well. One such implementation is shown in Figure 1(b).

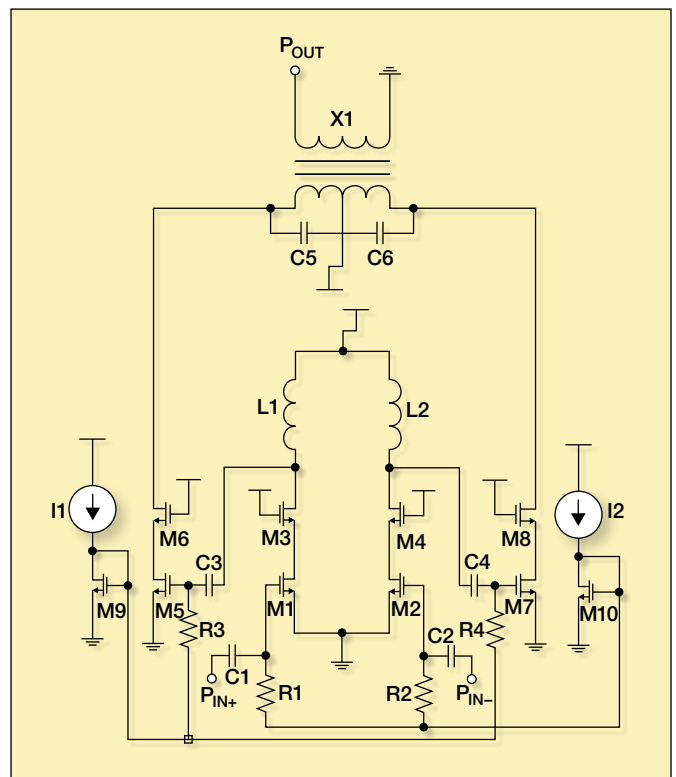


Figure 1(b). Cascode differential CMOS PA.



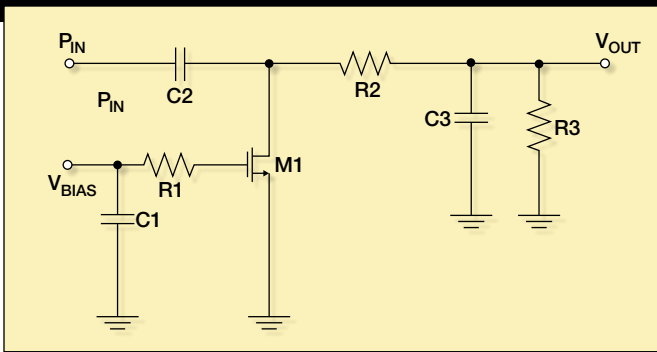


Figure 2. Power detector (PD) with a FET.

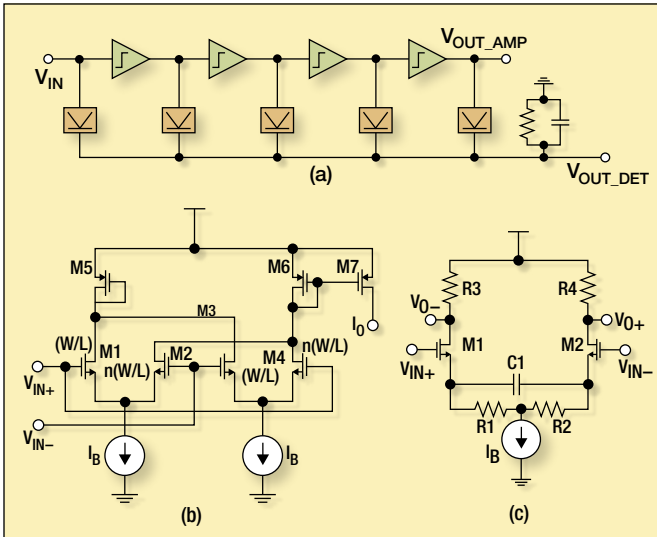


Figure 3. Log-amp-based PD.

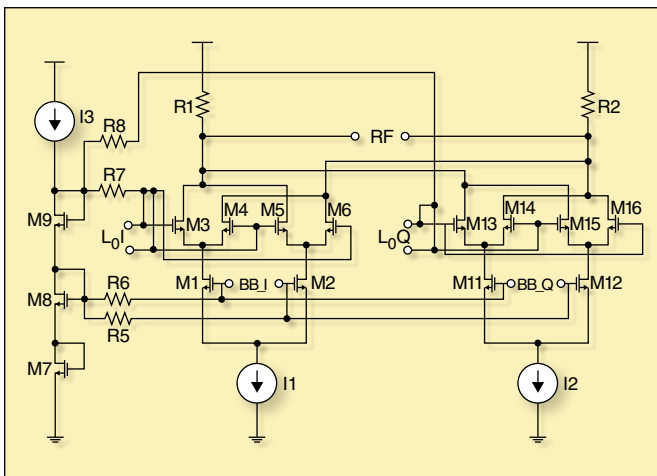


Figure 4. CMOS MOD.

Topology wise, it is similar to a cascode LNA. The advantage of the cascode configuration is to reduce the Miller multiply effect. Miller effect comes into play because of the parasitic capacitance between a FET's gate and its drain. In a common-source (CS) amplifier, it will be a problem. By inserting a common gate (CG) stage in the cascode configuration, the output and input are isolated. The input capacitance is also reduced. The additional advantage is more gain for the same amount of bias current since the bias current is reused. M1 through M4 are the driver stage while M5 to M8 complete the power stage. An integrated balun is used in this design since most widely used antennas in wireless devices are single ended.

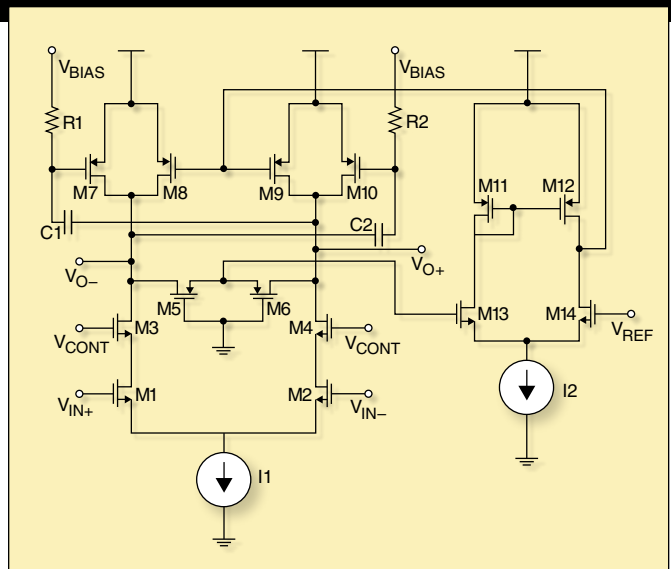


Figure 5(a). Variable transconductance AGC.

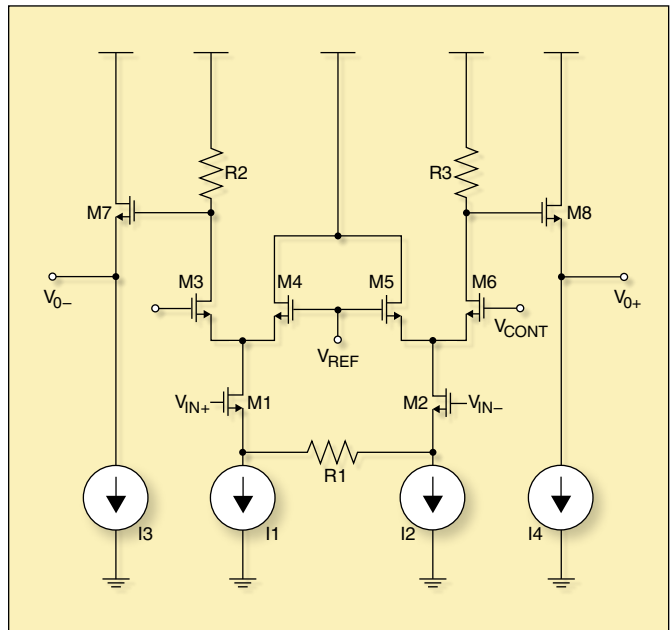


Figure 5(b). Variable biasing AGC.

A PD is used to monitor the PA's output power level. The PD's output dc voltage is fed back to the baseband for processing. A PD can be implemented in many ways. It could be as simple as a diode or a FET circuit. Or it could be as complicated as a circuit with hundreds of transistors. The level of complexity depends on the requirements for a PD. The important design parameters for a PD are dynamic range, linear-in-dB linearity, power consumption, ease of integration and its operating frequency.

A PD with one simple FET is presented in Figure 2. The basic idea is to use the square term of the active device. M1 is the active device. M1 is biased at the borderline between triode and saturation region. It means the  $V_{bias}$  or  $V_{gs}$  is set to be  $V_{ds} + V_t$ . The drain of the FET is close to zero. So if  $V_{gs}$  is slightly higher than  $V_t$  will bias M1 at the border line between the triode and saturation region. The standard equation for the drain current of a FET transistor in the saturation region is as follow:

$$i_D = \frac{K}{2} (V_{gs} - V_t)^2 \quad (1)$$



K is the device parameter that includes the physical dimensions of the device, electron mobility and oxide capacitance. Since  $V_{gs} = V_{ds} + V_t$ , then  $V_{ds}$  can be expressed as  $V_{ds} = V_{gs} - V_t$ . Equation 1 can be further simplified to:

$$i_D = \frac{K}{2} V_{DS}^2 \quad (2)$$

With equation 2, the square law relationship

between the input RF signal and output-rectified current is established. This is why the RF input is applied at the drain, not M1's gate. The rectified output current goes through load resistor R3 to establish the output voltage. R2 and C3 are the output filter. A FET can be configured in a common-source configuration as in an amplifier. It has the square law characteristics as seen in equation 1. But the  $V_t$  term will create an undesired dc offset term.

To get a high dynamic range (>60 dB), cascading the basic PD will extend the detection range. A popular and a high-performance implementation is the log-amp type. The generic multistages topology is illustrated in Figure 3(a). The basic building blocks are the limiter amplifiers, the rectifiers and a summer. The limiter amplifier has a rectifier at both the input and the output. The limiter's job is to provide gain and clip the output signal at a certain designed output level. The limiter amplifier nearest to the output port will clip first. Then stage by stage, the rest of the limiter will clip. A higher number of the gain stages will result in better linearity or linear-in-dB performance. The reason is each rectifier has a good linear power detection range. But the linear range is limited. By breaking up the total dynamic range into multiple numbers of linear regions, a piece-wise linear-in-dB approximation can be achieved. The limiter can be as simple as a differential amplifier with resistive load as shown in Figure 3(c). The rectifier is essentially a current rectifier as shown in Figure 3(b). The basic building block is an asymmetric differential amplifier pair. When  $V_{in}$  is small, most of the tail current flows through bigger FETs like M2 and M4. As  $V_{in}$  increases, the tail current is gradually steered into M1 and M3. So the output current linearly decreases as  $V_{in}$  is increased. Thus, a full-wave current rectifier is achieved.

The MOD is used to upconvert a baseband (BB) signal to the RF frequency. Since most modern wireless devices require both I and Q channels, two double-balanced mixers (DBM) are needed in a MOD. The implementation is illustrated in Figure 4. M1 to M6 is the DBM for I channel. M11 to M16 is the DBM for Q channel. Since the same DBM is used for both I and Q channel, only one DBM is discussed in detail. The incoming BB signal is amplified first by the gain stage such as M1 and M2. M3 to M6 are the switching FETs. It fundamentally serves the purpose of a multiply operation. In half the cycle, M3 and M6 are on. Local oscillator (LO) and BB signals are essentially multiplied in phase. In the other half of the cycle, M4 and M5 are turned on to reverse the polarity of the output signal. The output loads are implemented with resistors R1 and R2. The summer network can be simply done by routing both the I and the Q output current to the load resistor. The input stage can be configured in CG stage to avoid the voltage to current nonlinearity in the CS input stage.

There are many AGC topologies to choose from. The variable transconductance and the variable biasing AGC are the most popular for the high-frequency operation. The variable transconductance circuit is shown in Figure 5(a). It is based on the principle the transconductance of the FET changes as the FET goes

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from a saturation mode to a triode mode. Thus, the gain is varied. M1 to M4 can be considered as the typical differential cascode gain stage. The difference is that  $V_{cont}$  is applied at the gates of M3 and M4. As the  $V_{cont}$  decreases, the drain voltage at M1 and M2 drops. Eventually, M1 and M2 enters the triode region as  $V_{cont}$  is lowered to below  $V_{gs1} + V_{s1} - V_t$ . M7 to M10 are the current source type load. Thus, a common-mode feedback (CMFB) is needed to make sure the current source matches with the current sink I1. The common-mode voltage is sampled at the drain of M3 and M4 with M5 and M6. M5 and M6 can be considered as two large value resistors. They have the same value. The sampled voltage is fed to a comparator (M11 to M14). The reference is fed to one input M14 while the sampled common mode is fed to the other input M13. The error voltage is used to control the bias current out of the current source M8 and M9. M8 and M9 are the current bleeding path. The closed feedback loop ensures correct bias current follows with the desired reference voltage.

A variable current AGC is based on the idea that the transconductance of a FET changes with the bias current. By varying the bias current in the FET, the AGC can be accomplished. Such an implementation is presented in Figure 5(b). M1 and M2 are the input gain buffer. M4 and M5 are the current bleeding path. If  $V_{cont}$  is larger than the  $V_{ref}$ , more bias current flows through M3 and M6. In this mode, a high gain is expected. When the  $V_{cont}$  is reduced, more bias current flows through M4 and M5, the gain is thus reduced. M7 and M8 are the output emitter follower buffers to reduce output impedance. R1 is the degenerated resistor to improve the linearity of the AGC.

The CMOS VCO is based on the negative resistance theory. The NMOS-only version is presented in Figure 6(a). By cross coupling M1 and M2, a positive feedback is created in the circuit. Looking into the gate of M1 and M2, a negative resistance can be expected. The operating frequency is set by the resonant tank. L1 and L2 provide the inductance part. The frequency can be tuned coarsely by the capacitance bank and fine tuned with the varactor capacitance. In Figure 6(a), two bit four states capacitance banks are used. More banks can be added if a larger process variation is expected. By turning on/off M7 and M8, more/less total capacitance can be expected in the resonator tank. The varactor is implemented with FETs M5 and M6 by tying the source and the drain. M3 and M4 are the output buffers. Complementary CMOS VCO is presented in Figure 6(b). The key change is to add a cross-coupled PMOS pair. By adding a PMOS pair, two more elements are added to contribute the negative resistance while the bias current remains the same. So it is more power efficient.

## Summary

Each major building block in a highly integrated Tx is discussed in this article. The circuits are generic enough to be adopted in most wireless applications. This article offers a good starting point for your next Tx RFIC design. **RFD**

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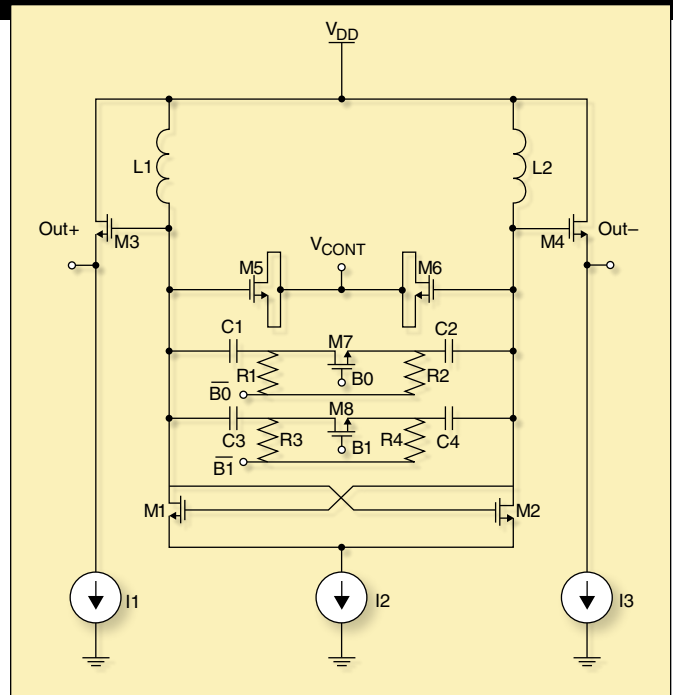


Figure 6(a). NMOS-only VCO.

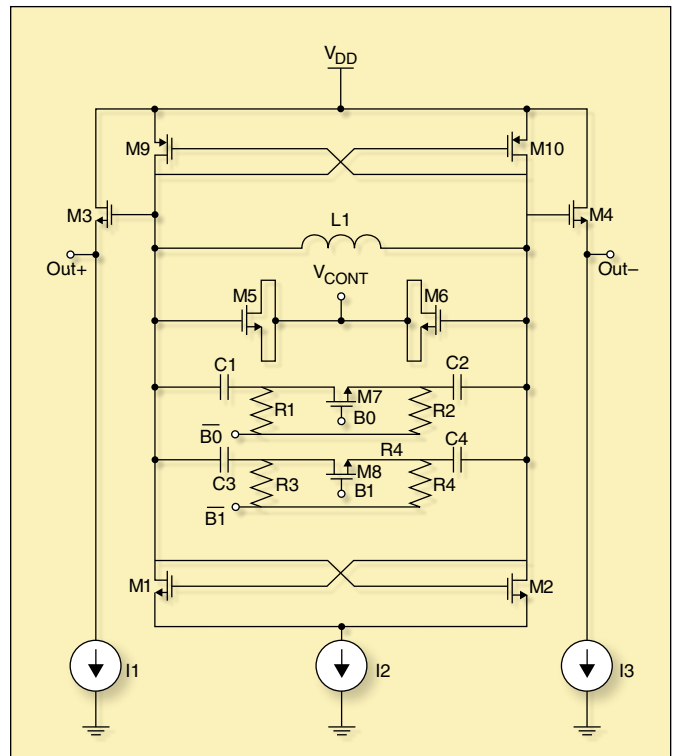


Figure 6(b). Complementary CMOS VCO.

## ABOUT THE AUTHOR

Louis Fan Fei is currently an RF engineer at Garmin International, Olathe, KS, where he has been designing GPS receivers since 2003. He worked on WLAN and wireless local loop circuits at Lucent/Agere System from 1998 to 2003. He received his BEE and MSEE from Georgia Tech in 1996 and 1998, respectively.