

# Understanding state of the art in ADCs

The article investigates key parameters that enable users to choose the right ADC based not only on performance, but cost and other tangible and intangible aspects of converters.

By Brad Brannon

There are many dimensions of performance to analog-to-digital converter (ADC) technology. Some of which are listed in Table 1. These are common metrics for which ADCs may be selected and have value for certain areas of interest.

Until the late 1980s, military requirements tended to drive data-converter markets. Military needs were driven by radar, communications applications and EMP<sup>(1)</sup> detection. Often these converters were pushed in a single dimension of performance such as spurious-free dynamic range (SFDR) or sample rate. Occasionally, two dimensions may have been maximized, but rarely was this the case in multiple dimensions of performance. In fact, many of these dimensions were unimportant and were often sacrificed for the needed performance specification.

Today, designers, especially in commercial applications, expect multiple dimensions of converter performance, in many cases, up to four or five. Therefore, parameters such as power consumption, SNR, SFDR, input bandwidth and cost must all be optimized. High-speed converters once reserved for military and perhaps high-end test equipment are finding applications in industrial and consumer products. Notable applications include cellular infrastructure<sup>(1,2)</sup> and a plethora of other wireless and wired applications such as DOCSIS, Wi-Fi, WiMAX and high-end consumer commercial broadcast receivers for HD, FM, AM and satellite broadcasts. The broad appeal for a well-rounded ADC is rooted in the fact that once the signal band of interest is digitized, signal processing can be optimized and tailored for nearly any application using software techniques as found in software-defined radio (SDR) or software-defined instrumentation.

## ADC performance

As software-defined systems become more common, performance expectations for converters continue to increase, generally remaining one step ahead of actual converter performance. In general, significant upward pressure exists on SNR and SFDR and downward pressure on pricing. To a large degree, these market pressures are working as SNR performance is experiencing performance jumps not entirely predicted by reports by Walden<sup>(3)</sup> and Le, et al.<sup>(4)</sup> and others as a direct result of customer drive and increasing competitive pressures. Although not without performance penalties, cost for converters is falling as designs

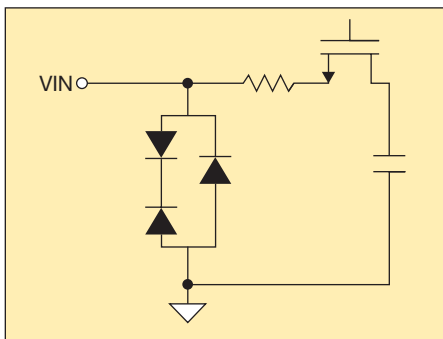


Figure 1. Typical ADC input network.

Table 1. Sampling of dimensions of ADC performance.	
Dimension of performance	Value
• SNR	Sensitivity to small signals
• SFDR, harmonics and intermodulation	Rejection of undesired interferers
• Power	Portability or low cost of supplies
• Bandwidth	Fewer radios to capture intended signal range
• Sample rate	Capture of fast transients or large bandwidths
• Cost	Low cost radios

are moving from proprietary semiconductor processes to industry-standard CMOS processes that are generally much less expensive. Initially, SNR performance dropped back by as much as one-half of a bit during this process transition but recent improvements show signs that performance on standard CMOS processes are back in line with proprietary processes. SFDR is experiencing a slightly different trend. Performance for high-end ADCs has stalemated over the last few years and has experienced little forward progress indicating that basic linearity performance has not improved over the last few years. In order to move SFDR performance forward, a displacing technology will be required.

While performance will continue to improve in the varied dimensions, end users can affect the pace that these improvements occur by providing performance feedback to ADC manufacturers. Only when designers know exactly which specifications to target will they know how to optimize the designs, trading off one performance for another in a meaningful and useful manner.

## What are the requirements?

While there are many dimensions of performance, there are always a few key specifications of interest. These specifications are key to a broad range of applications and offer a view into widely accepted parameters and how they enable certain features as well as how they interact with other parameters.

## Wider input bandwidth

Converter bandwidth is largely determined by the size of the sample capacitors used in the ADC. Bandwidth is inversely proportional to the value of the sample capacitor as shown in equation 1. This is easily observed by considering that the sample process consists of a finite resistance sample switch and a sample capacitance. In this case, it is readily apparent that bandwidth is determined by the combination of the switch resistance (and any external series resistance) and the sample capacitor. Therefore, to maximize input bandwidth, both R and C should be minimized (Figure 1).

$$BW \propto \frac{1}{C}$$

Wider input bandwidth allows for better slew rate performance and more accurate tracking of fast slewing analog signals associated with both transient events and high-frequency sinewaves. It also allows wideband analog signals to be accurately sampled and is often accompanied by a faster sample rate.

Conversely, wider input bandwidth allows more noise to pass the ADC input stages and be digitized, resulting in lower SNR than would have for a lower-bandwidth ADC. This is the reason many high-bandwidth ADCs have lower SNR performance than otherwise predicted. If the sampling rate is high enough the input noise will be widely distributed across the Nyquist band and digital filtering can remove excess noise should the desired bandwidth fall within a Nyquist band of the ADC. However, if the sample rate is much less than the analog input center frequency the input noise will be aliased into the Nyquist zone and the noise density can become quite high. Therefore, great care must be taken both in the design and use of wide bandwidth ADCs.

In reality, wider bandwidths are only necessary for wideband signals such as transient events. High-frequency sampling only needs sufficient bandwidth to sample the signals of interest. Since most common signals are band-limited both for performance and regulatory reasons, 'wider' bandwidth is not a necessary requirement of IF undersampling. Because of this, a class of ADCs called bandpass converters allow high-frequency signals to be digitized without the excess bandwidths. This results in low-distortion sampling and high SNR performance in the signal band of interest. These are typically found as bandpass delta-sigma converters and are often used in highly integrated receiver functions such as those used in Wi-Fi chipsets. Other examples for more general-purpose usage can be seen in products like the AD6600 (Figure 2). Its noise improvements are achieved by allowing the internal analog network to be resonated at the desired IF to improve unit SNR and to provide rejection to signals outside the band of interest. Standard converters may also be resonated for improved performance, reducing the drive requirements, improving noise performance and filtering input spurious<sup>[5]</sup>.

### IF undersampling

The IF undersampling technique has long been sought as a means for reducing the complexity of a receiver design. In fact, sampling as close

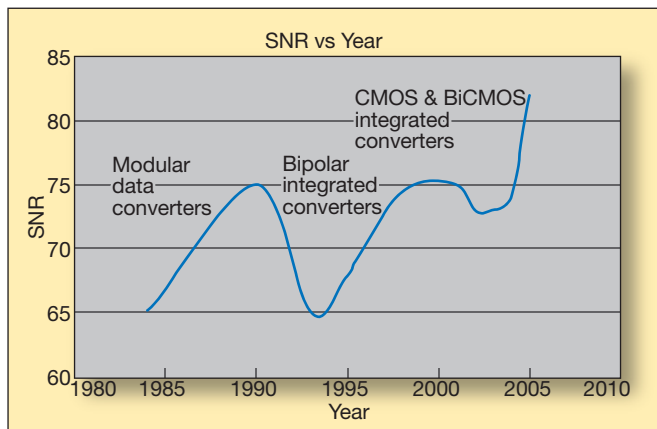


Figure 3. Recent SNR trends in high-speed Nyquist converters.

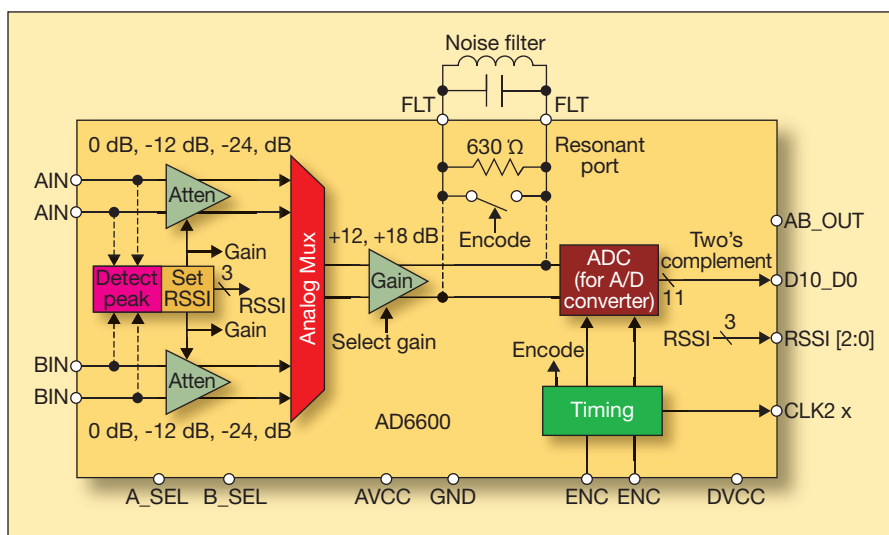


Figure 2. Example of a bandpass ADC for general-purpose use.

to the antenna as possible offers the possibility of reducing the size and complexity of the receiver function in a system. Most modern cellular base stations implement IF sampling allowing one or more IF stages to be eliminated from their system reducing both cost and complexity.

While IF undersampling does reduce overall system cost, there is a performance trade off in that IF undersampling ADCs in the past have generally resulted in lower performance than baseband sampling ADCs. Over the past few years, this requirement has driven the demand for high-performance IF sampling ADCs and are now available that are optimized for both SNR and SFDR for frequencies as high as 450 MHz.

### Sample rate

Sample rates are driven by several factors. The largest driver is to have a sample rate that is an integer multiple of common data rates for communication standards. For example, CDMA2000 has a base symbol rate of 1.2288 MHz, WCDMA has a base rate of 3.84 MHz and TD-SCDMA has a base rate of 1.28 MHz. Based on these rates, common sample rates of 78.6, 92.16, 122.88 and 245.76 megasamples per second (MSPs) are common. As in the past, the ADC technology determines the preferred sample rate. And over the past few years, the preference is to run above 80 MSPs in most new designs.

Higher sample rates do improve noise performance of ADCs. While the overall integrated noise does not improve, the distribution of the noise over wider bandwidths does offer improvements in noise spectral density (NSD). The lower the noise spectral density, the more sensitive a receiver can be designed. This process is often referred to as processing gain and is nothing more than distributing the same noise over a wider band of frequencies and then digitally filtering out the noise in the frequency bands that are not of interest. Doubling the sample rate can improve the noise spectral density by a factor of 3 dB resulting in a significant improvement in performance of many systems.

However, there are limits to how much sample rates can be increased. Current FPGA<sup>[1]</sup> and ASIC<sup>[1]</sup> technology limits CMOS<sup>[1]</sup> data rates to about 250 MHz, LVDS<sup>[1]</sup> to approximately 800 MHz and PECL<sup>[1]</sup> to approximately 1.5 GHz. Other logic schemes such as CML<sup>[1]</sup> offer the possibility of even higher rates. While some applications have moved to LVDS and PECL, the bulk of applications are implemented in CMOS. This will change in the future, but for now, the mainstream driving applications are still CMOS.

### Dynamic range and noise

As already established, noise level is directly proportional to input bandwidth (SNR is inversely proportional to bandwidth). As seen in

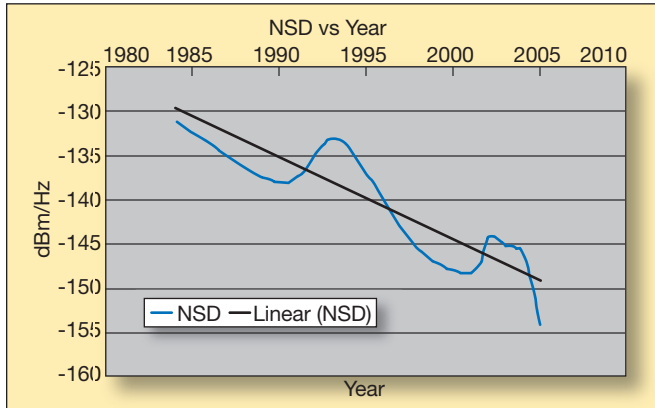


Figure 4. Noise spectral density (NSD) trends for production high-speed Nyquist converters.

equation 2, noise is proportional to Boltzmann's constant and absolute temperature and inversely proportional to the sample capacitor.

$$\text{noise} \propto \frac{kT}{C}$$

As stated earlier, noise density decreases with sample rate. As both SNR and sample rate improve, the thermal noise floor continues to reduce. While a long way from device thermal noise, current wideband converters are approaching the noise level of an optimally matched antenna (-174 dBm/Hz) making them easier to use in systems with even modest conversion gain. Current technology is within 20 dB of reaching this threshold and new techniques are being discovered for reducing the noise level through signal processing and better analog design. Figure 3 depicts recent SNR trends in high-speed Nyquist converters, while Figure 4 shows a similar trend for NSD.

In most applications, this level of performance is only achieved when using a low jitter clock source<sup>[6,7]</sup>. In recent years, low jitter oscillations, PLLs, DDS and other devices<sup>[8]</sup> have become available that can both clean up reference clocks and provide high fan outs to multiple devices in a system. Current ADC technology provides clock jitter as low as about 50 fs creating quite a challenge to system clock designers. Only when system designers provide clock jitter this low can full performance be expected from ADCs, especially when operated at high IFs.

### Spurious performance

Better spurious performance is achieved by wider bandwidth. A system with a large input bandwidth is less prone to slew rate limitations, allowing the ADC to better track the signal input to the device. As seen in equation 3, bandwidth is proportional to  $1/C$  and since a fast slew rate translates to spurious performance, the same  $1/C$  relationship applies.

$$\text{Spurious} \propto BW \propto \frac{1}{C}$$

Therefore, for optimal spurious performance a wide input bandwidth is desirable. This means the sample capacitance must be as small as possible. However, from equation 2 we know that making the sample capacitance small, the increased input bandwidth allows more noise to enter the front end of the ADC and be spread across the Nyquist spectrum. Thus, SNR and SFDR must always be traded off between one another. Academic literature has continually produced work that explores the key to significantly improved performance. The studies examine how to improve the sampling switch mecha-

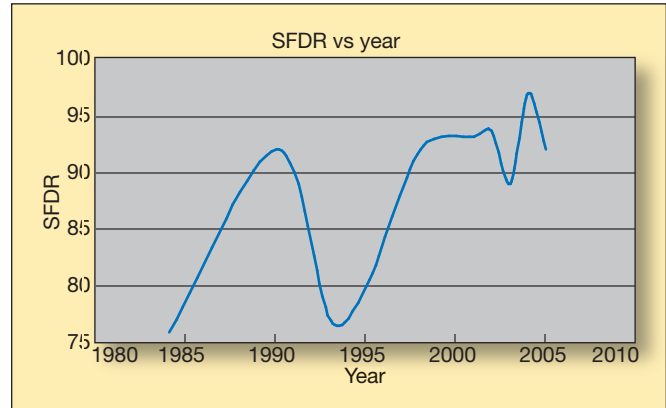


Figure 5. Baseband spurious performance trends for production high-speed Nyquist converters.

nism while optimizing both a reduced sample resistance and smaller capacitor<sup>[9]</sup>. Figure 5 reflects the performance improvements in SFDR over the years.

Given the trends for both SNR and SFDR, how do they stand up against system requirements? Table 2 shows required performance by air interface for popular wireless standards. These specifications are for wideband multicarrier performance without the benefit of automatic gain control, similar to what would be required for a software-defined receiver capable of processing that standard. As seen, GSM/EDGE in the 900 MHz band is the most challenging and currently not possible with existing converters (current systems utilize single-carrier design with narrowband filters and AGC). Referencing Figures 3 and 5 clearly shows that for the remaining standards, multicarrier SFDR is entirely possible from an ADC perspective.

### Common platforms and reuse

Unlike digital designs where Moore's Law<sup>[10]</sup> is cited, analog and mixed-signal designs cannot constantly be shrunk to take advantage of smaller geometry processes. There are at least two fundamental process limitations. Unlike digital designs, analog blocks are not designed in verilog but instead optimized at the transistor level for the specific process to optimize power, noise and linearity. When moved to a new process, the optimization must be completely redone. In fact, many times, totally new design topologies are required, forcing new designs and architectures. In addition, some processes are simply not compatible with analog signal processing and variations must be made.

Design reuse is similarly limited to product variants or derivatives on the same process. It is not possible to take one 0.35  $\mu\text{m}$ -based design and migrate it to 0.18  $\mu\text{m}$  and expect performance to be the same or better. In general, it takes a few product generations for designers to understand the performance curves of a new process and advance the performance curves for high-speed ADCs. As stated, using the larger transistors on the finer line process will waste expensive die space and probably will no longer be optimized. Designing product derivatives or close variants are highly possible within the same process. In fact, this is often seen in products where single, dual, quad and octal channels are required. Likewise, reuse is seen in cases where integration with

Table 2. Required performance for popular wireless standards.

Standard	SNR	SFDR	Sample rate
• TD-SCDMA	73 dBFS	83 dBFS	122.88 MHz
• CDMA2000	79 dBFS	86 dBFS	92.16 MHz
• WCDMA	70 dBFS	81 dBFS	92.16 MHz
• WiMAX	~75 dBFS	~90 dBFS	80 MHz
• GSM/EDGE (900 MHz multicarrier)	85 dBFS	110 dBFS	104 MHz



additional analog and digital features is required. At the design core level (fully functional ADCs) products like ADI's AD9228 12-bit 65 MSPS quad ADC are easy to reuse across a large portfolio of both standard products including octals and more application-specific products that could include gain, filtering and mixing analog functions. At the circuit level, functions such as output drivers, references and amplifiers are easily reused as long as the processes remain the same.

Likewise, mixed-signal ICs never follow the same cost reduction as experienced with digital chips. Once a product is released, its design is fixed and forever tied to that process geometry. A common method to reduce the cost (and price) is to improve product yield and increase volume or to design a new ADC on a new, lower-cost process. Unfortunately, this results in a reduction in performance over previous generations. While this does correct in future generations, jumping processes frequently results in reduced performance from one device to the next.

When devices are migrated to new processes, it is often the desire to make the new device pin and function compatible. Unfortunately, it may behave differently in a number of ways. Not only will dynamic performance be different as outlined above, but analog inputs (range and impedance) and digital output characteristics may be different. More important, newer processes typically have smaller breakdown voltages and, therefore, support lower supplies. While most processes do have the ability to retain supplies of their previous generation, maintaining supplies from two or more generations is becoming increasingly difficult as geometries continue to reduce. These issues make it almost impossible for pin-compatible drop-in replacement for the older device without changes to supplies, input matching networks and receiving logic gates.

With the introduction of 0.35  $\mu\text{m}$  CMOS converters, the inclusion of digital features to the core ADC offer many interesting functions beyond the standard output data format. New feature sets include shuffling, dithering, output test patterns, built-in self test and a plethora of other user features<sup>[12]</sup>. However, accessing these features can be problematic. Many new high-speed converters now offer SPI interfacing to access the rich features sets once reserved for slow-conversion ADCs. Because these features are digital, they can now be easily transported from one design to the next, even across process changes because of their generation in Verilog or other digital language. Over time, many of these new features will emerge as 'standard' features of high-performance ADCs and will exist for many generations, even through process shrinks and changes.

### What are the limitations?

A number of limitations exist in data converters. As mentioned, there is a natural conflict between SNR and SFDR. These conflicts are improved by advances in architecture and optimizations in process. While improvements have continually occurred over time, the process is at least partially reset each time a new semiconductor process is employed. Because of this, improvements often tend to be two steps forward and one step backward. Cost pressures push decisions to switch to newer processes whereas remaining on older processes would indicate that generational improvements in performance are possible but not necessarily a cost reduction.

Additional issues exist with moving to smaller geometries. As the geometry sizes decrease, breakdown voltages are reduced making it harder to design for performance. In terms of SNR where thermal noise may be considered 'finite' for a process or architecture, larger input swings can improve performance. If breakdown voltages constrain signal swing, SNR limitations may result. While this is not a problem for low-resolution converters, it is a big limitation for high-resolution converters, especially those with large input bandwidths. Similarly, lower breakdown devices offer only reduced overhead between analog signal swings and power supplies, implying poorer linearity from those devices. In summary, smaller geometries with lower breakdown values offer poorer noise and linearity performance.

Interfacing to the analog input is becoming more difficult. For low-frequency applications, this is not a big issue but as IF frequencies increase and direct RF sampling becomes a possibility, proper impedance matching to the source becomes more critical. At high frequencies, optimal ADC performance is only achieved when a proper match exists not only because the input is presented with a maximum of signal level but because ADC input behavior in terms of both noise and especially spurious is optimized<sup>[5]</sup>.

### Where are we headed?

Clearly, SNR is on an improving trend. Based on noise spectral density, performance over the last 20 years indicates a solid 1 dBm/Hz per year. As for spurious, this report has provided antidotal evidence showing that SFDR performance has been constant for the last five to 10 years in the baseband region. While there is a clear need for full-scale performance in the range of -110 to -120 dBFS, consistent performance of only -95 to -100 dBFS is available in the baseband region today. At the same time, great attention has been paid to increasing SFDR performance in the mid and high IF regions with a result that usable IF frequencies as high as 450 MHz are not uncommon for some applications.

In addition to improvements in the analog signal path, improvements in the digital domain can also improve performance. With digital features such as shuffling, dithering<sup>[13]</sup> and calibration becoming standard features on high-speed converters, it is clear that the 'D' is getting bigger in ADC. Each of these digital techniques has the ability to improve the linearity and noise performance of the converter under a variety of conditions.

In addition to improvements in process and Nyquist converters as described here, advances in other classes of converters holds potential and may displace these converters in some applications. As mentioned, another key to improved performance is improved clock sources. To achieve rated SNR, especially at high input frequencies, clock jitter must be minimized.

In the end, it is not just the ADC designer who is challenged to design a better ADC; the system designer is challenged to blend all of these aspects together. One must choose the right ADC based not only on performance, but cost and other tangible and intangible aspects of converters. **RFD**

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